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ALPHA

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Deliverable 3.5
Experimental results on new gateway functions implemented with commercially available modules

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Executive Summary

The adaptation of the Residential Gateway for using the Gigabit Ethernet transceivers for Plastic optical fibre is described. The adaptation is performed using off-the-shelf devices and with minimal architecture changes.

A hybrid solution for transferring a part of the QoS functionality of the home server to the Residential Gateway has been proposed. Preliminary experimental (testing) results have been described.

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1 Introduction

1.1 Purpose and Scope

Goal of this document is to provide an overview of the experimental characterization of new functionalities devised for the residential gateway in the scope of the ALPHA Project.

More in detail, the document is focused on providing:

- details on the new functionalities
- details on how such functionalities are implemented on the residential gateway, both from the hardware and software point of view
- first experimental results on the new functionalities, obtained in the development labs of the involved partners during 2009
- plan for demonstration of the new functionalities in the official testbeds during the third year of the project (2010)

The new functionalities which are the core of this document are:

- Integration on the Residential Gateway of 1 Gbps Plastic Optical Fibre (POF) transceivers
- Porting on the Residential Gateway of UPnP QoS functionalities

These features are described in following sections; further details can be found in the Milestones of Task 3.5.

1.2 Reference Material

1.2.1 Reference Documents

[1]	Milestone 3.8, ALPHA Project
[2]	Milestone 3.9, ALPHA Project
[3]	Home Gateway Technical Requirements: Residential Profile; Version 1.0, 29/04/2008, Home Gateway Initiative
[4]	Deliverable 3.1, ALPHA Project
[5]	Deliverable 4.3, ALPHA Project
[6]	Milestone 3.10, ALPHA Project
[7]	UPnP-QoS Architecture:3 For UPnP Version 1.0; 30/11/2008, available online at: http://www.upnp.org/specs/qos/UPnP-qos-Architecture-v3.pdf
[8]	Deliverable 5.1, ALPHA Project
[9]	Deliverable 5.3, ALPHA Project
[10]	Deliverable 1.1, ALPHA Project

1.2.2 Acronyms and Abbreviations

AC	Alternating Current
ACS	Auto Configuration Server
AFE	Analog Front End
AGC	Automatic Gain Control
AN	Access Network
ASIC	Application-Specific Integrated Circuit
ATA	Analogue Terminal Adapter

ATM	Asynchronous Transfer Mode
BER	Bit Error Rate
BSD	Berkeley Software Distribution
BW	Band Width
C&M	Control & Management
CAC	Connection Admission Control
CLI	Command Line Interface
CML	Current Mode Logic
CP	Control Point
CPE	Customer Premises Equipment
CWMP	CPE-WAN Management Protocol
DDR	Double Data Rate
DHCP	Dynamic Host Configuration Protocol
DIY	Do It Yourself
EBI	External Bus Interface
ECL	Emitter Coupled Logic
Enet	Ethernet
ETH	Ethernet
EXT	External
FEC	Forward Error Correction
FXO	Foreign eXchange Office
FXS	Foreign eXchange Subscriber
GMII	Gigabit Media Independent Interface
GND	Ground
GPIO	General Purpose Input/Output
GPOF	GigaPOF
GW	Gateway
HD	High Definition
HG	Home Gateway
HN	Home Network
HW	HardWare
ICMP	Internet Control Message Protocol
ID	Identifier
IEC	International Electrotechnical Commission
IGMP	Internet Group Management Protocol
IMS	IP Multimedia Subsystem
IP	Internet Protocol
IPsec	Internet Protocol Security
ISO	International Standards Organization
Java VM	Java Virtual Machine
JTAG	Joint Test Action Group
L1	Layer 1
L2	Layer 2
L3	Layer 3
LAN	Local Area Network
LC	Local Connector
LED	Light Emitting Diode
LLC	Logical Link Control
LVDS	Low Voltage Differential Signaling
MAC	Medium Access Control
MIM	Management Information Model
MLT	Multi Level Transmit

MMF	Multi Mode Fibre
MOST	Media Oriented Systems Transport
MPI	Multifunction Peripheral Interface
NAND	Not AND
NAPT	Network Address and Port Translation
OSGi	Open Service Gateway initiative
OSI	Open Systems Interconnection
P2P	Point-to-Point
PC	Personal Computer
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCM	Pulse Code Modulation
PHY	PHYsical layer
PHY-TC	PHY-Transmission Convergence
POF	Plastic Optical Fibre
PPP	Point-to-Point Protocol
PPPoE	PPP over Ethernet
PSTN	Public Switched Telephone Network
PTH	Place Through Hole
QD	QOS Device
QM	QOS Manager
QOS	Quality Of Service
QPH	QOS Policy Holder
RAM	Random Access Memory
RF	Radio Frequency
RG	Residential Gateway
RIP	Routing Information Protocol
RJ	Registered Jack
RTCP	Real-time Transport Control Protocol
RTP	Real-time Transport Protocol
SC	Simple Connector
SDK	Software Development Kit
SerDes	Serializer Deserializer
SFF	Small Form Factor
SFP	Small Form-factor Pluggable
SHL	Shield
SIP	Session Initiation Protocol
SLAC	Subscriber Line Audio-processing Circuit
SLIC	Subscriber Line Interface Circuit
SMA	Sub Miniature A
SMD	Surface Mounting Device
SMF	Single Mode Fibre
SMI	Small Media Interface
SNMP	Simple Network Management Protocol
SNR	Signal-to-Noise Ratio
SOAP	Simple Object Access Protocol
SPI	Serial Peripheral Interface
ST	Straight Tip
SW	SoftWare
SYSLOG	SYStem LOG
TCP	Transmission Control Protocol
TELNET	TELecommunication NETwork

TFTP	Trivial File Transfer Protocol
TOS	Type Of Service
TOSLINK	TOShiba LINK
TR-069	Technical Report 069 (aka CWMP)
TX	Transmitter
UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol
UPnP	Universal Plug-n-Play
USB	Universal Serial Bus
UTOPIA	Universal Test and Operations Physical Interface for ATM
VoIP	Voice over IP
VPN	Virtual Private Network
WAN	Wide Area Network
WebUI	Web User Interface

1.3 Document History

Version	Date	Authors / Editors	Comment
01	2009-11-19	M.Giltrelli	ToC
02	2009-11-24	M.Giltrelli, L. D'Ascoli	Contribution to chapter 2 included
03	2009-12-14	G. Bettoni	Luceat contribution to chapter 3 included
04	2009-12-16	M. Giltrelli, F.Chino	Telsey contribution to chapter 3 included
05	2009-12-17	J. Nelis, M. Giltrelli	Contribution on UPnP QoS partially included
06	2009-12-21	G. Bettoni	Luceat contribution to chapter 3 included
07	2009-12-23	M. Popov	Preliminary review of the document
08	2010-01-06	J. Nelis	IBBT contribution to chapter 3 updated
09	2010-01-07	M. Giltrelli	Contribution to chapter 4 included
10	2010-01-11	M. Giltrelli, L. D'Ascoli	Contribution to chapter 5 included
11	2010-01-11	M. Giltrelli, M. Pegorer	Contribution on UPnP QoS experimental results included
12	2010-01-12	G. Bettoni, M. Giltrelli	Contribution to POF module experimental results included
13	2010-01-13	M. Pegorer, M. Giltrelli	Finalised contribution to UPnP QoS experimental results
14	2010-01-13/15	G. Bettoni, M. Giltrelli, F. Chino, M.Popov	Finalised contribution to POF experimental results + final check

2 Residential Gateway Overview

Goal of the chapter, is to provide a brief overview of the key elements of the architecture of a Residential Gateway (RG), as previously described in [1], [2].

Figure 2.1 depicts the functional architecture of the RG: in particular, the picture emphasizes the Wide Area Network (WAN) interface on the left; also referred to as Access Network (AN) and the Local Area Network (LAN) interfaces on the right; also referred to as Home Network (HN). In the figure, alongside with the interfaces, also the respective OSI stacks are shown, plus the voice and USB interfaces.

Furthermore, the picture illustrates many of the internal functionalities of the RG itself, for instance Access Control functionalities, Remote Access, and such.

Finally, the figure shows also the Data Interoperation plane and the related functional connections, alongside with the Control Interoperation and the Management Interoperation planes.

Further details can be found in [1], [3].

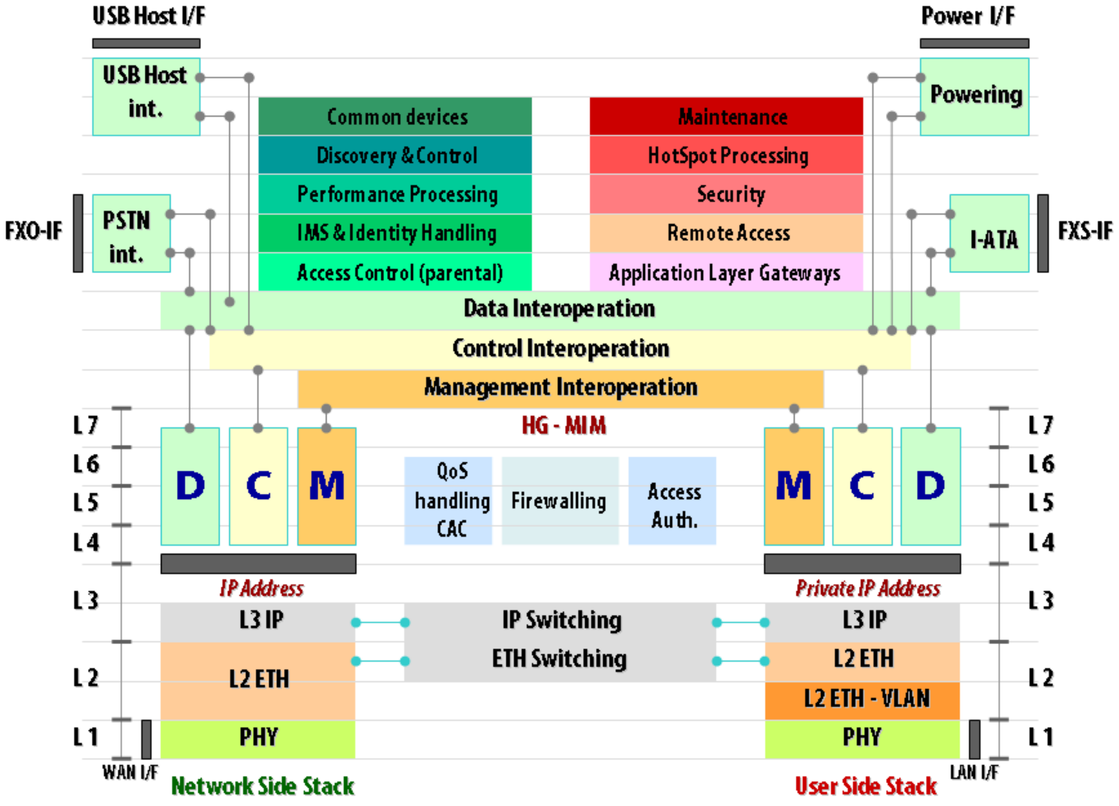

Figure 2.1 – Residential Gateway functional Architecture; AN is on the left side of the picture, HN on the right.

In Figure 2.2 is shown the architecture of the RG in terms of physical connectivity, with the exception of the USB interfaces; alongside with the somehow "classical" interfaces of a gateway devoted to the residential user that comprise Ethernet, Wi-Fi and USB connectivity, *is shown also the Plastic Optical Fibre (POF) interface that is a new feature specifically dedicated to the ALPHA gateway*. Further details concerning the POF module implementation will be given in the following sections.

As can be seen from the picture, all the different arms of the RG devoted to a specific interface share the same common building blocks: in fact, each arm is terminated with the proper PHY interface, that can be electrical (for the copper Eth ports and the FXS ports), optical (for the POF ports) or radio (for the Wi-Fi); each PHY block interoperates with the PHY-TC block, which translates from the PHY specific format to the Ethernet format internally to the RG (and vice versa); the Ethernet packets are then forwarded to the LLC-MAC block that handles the interoperability with the higher levels of the OSI protocol stack.

In the same picture, it is easy to spot that also the interface on the WAN side of the device hosts a set of building blocks that implements the same functionalities; as a last remark on the picture, the internal switch that allows the intercommunication among the different interfaces and the Residential Gateway controller (also referred to as Network Processor) are also shown.

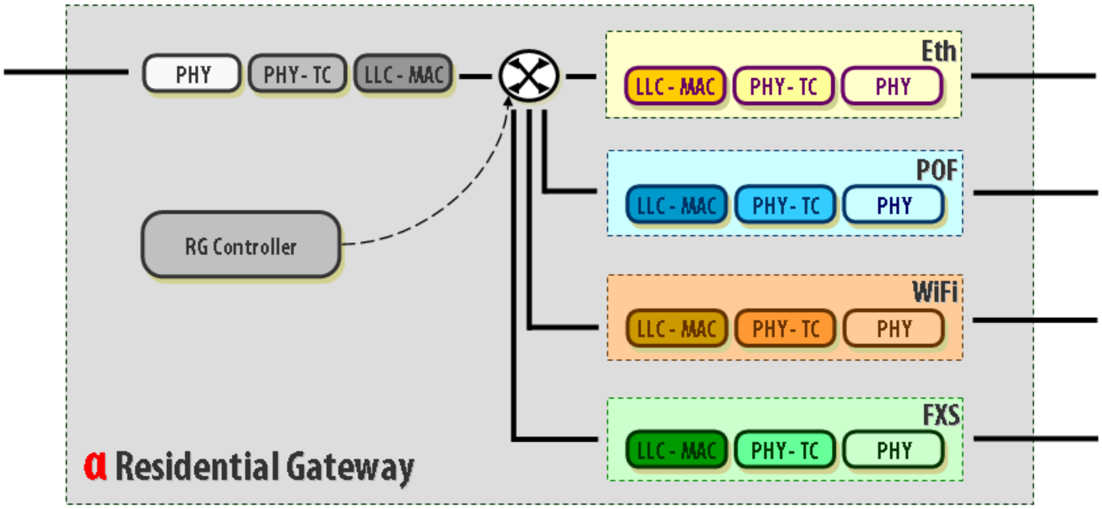

Figure 2.2 – RG physical architecture; AN is on the left side of the picture, HN on the right.

2.1 Hardware specifications of commercially available RG

Following the ALPHA Project Technical Annex (Annex I), the ALPHA specific Residential Gateway will be implemented via the use of commercially available components; as a consequence, the ALPHA specific features will be hosted on an off-the-shelf RG platform[1]. Such a platform is briefly described in this and the following section.

The hardware architecture of the available RG platform is depicted in Figure 2.3: the Access Network is on the right side of the picture (the fibre uplink), while the other connections belong to the Home Network domain.

As depicted (and anticipated), the gateway is provided with a fibre uplink for WAN access; concerning the LAN side connectivity, the device provides 4 Fast Ethernet ports, a Wi-Fi 802.11 b/g/n interface, a couple of USB host ports and an integrated VoIP module, capable of handle 2 voice lines.

Comparing straightforwardly Figure 2.2 and Figure 2.3, it is possible to identify the same functional blocks in both pictures, in particular the switch, the Ethernet, Wi-Fi and FXS interfaces, and the controller/processor; the block diagram of the ALPHA gateway shows also the POF module, which is of course not present on the commercial device, while the latter highlights also the presence of the USB interfaces, which are however not relevant for the applications devised in the project.

In Figure 2.4 is shown, for sake of completeness, the port functional connectivity of the RG shown in Figure 2.3.

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[1] In general only ALPHA relevant functions will be actually configured and made available.

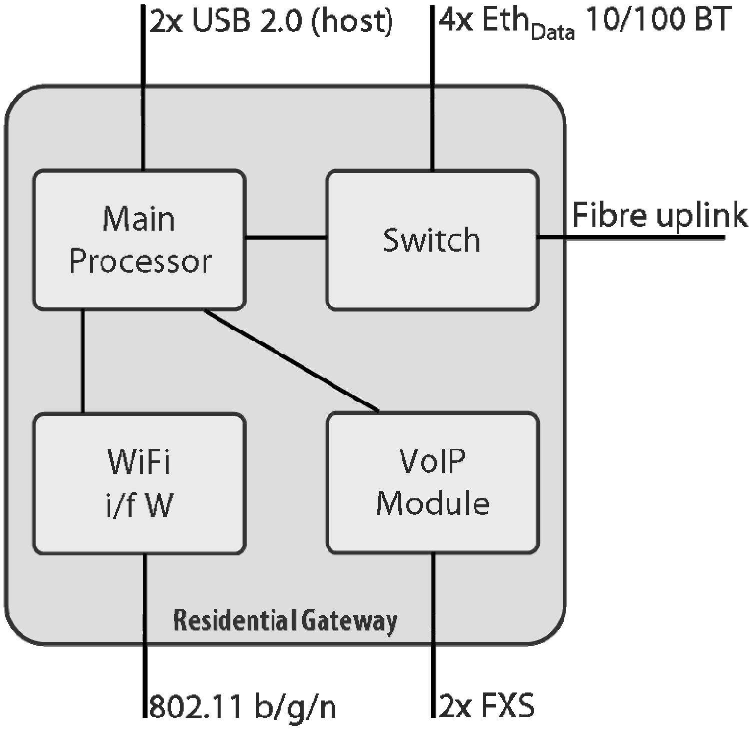

Figure 2.3 – Commercially available RG's architecture

As anticipated, the commercially available RG will serve as a base to develop the ALPHA RG; therefore, its HW will have to be customised accordingly: details will be given in the relevant sections.

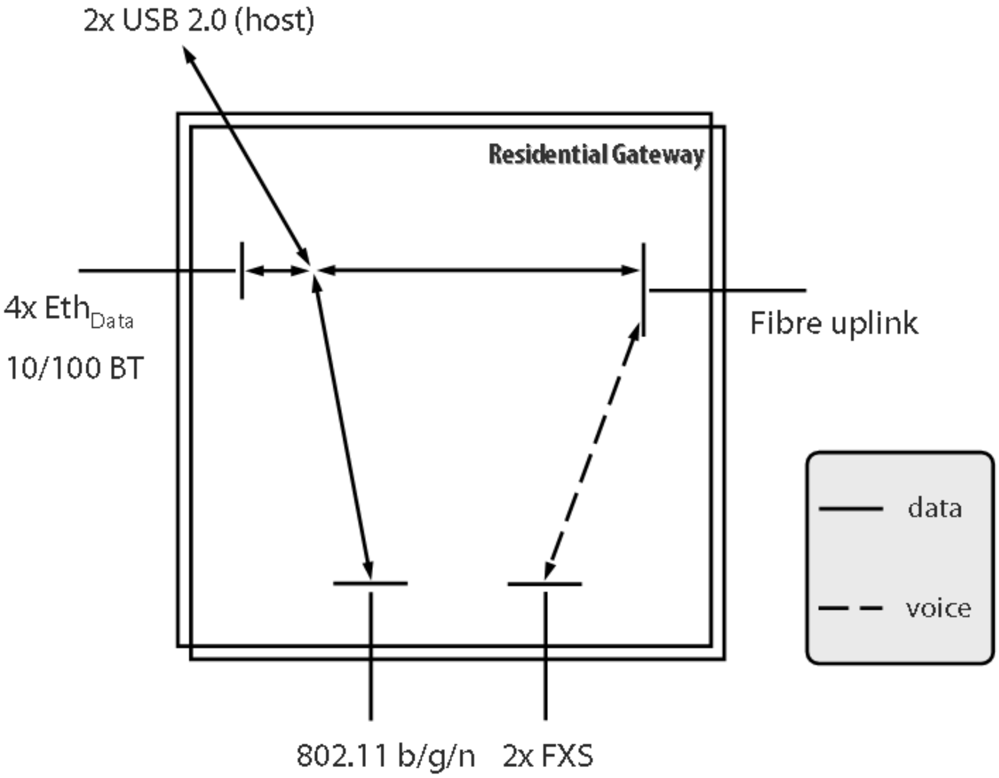

Figure 2.4 – Commercially available RG's port functional connectivity

2.2 Software specifications of commercially available RG

The functional architecture of the SW platform of the commercially available RG is outlined in Figure 2.5; it is not the scope of this document to go into details concerning the architecture of the RG; however, from a quick examination of the picture it is possible, to identify the software modules deputed to the handling of the physical blocks shown in previous pictures and specifically to the management of the different interfaces (Ethernet, Wi-Fi, USB and FXS).

In the upper part of the picture the different protocols used by the RG itself to implement its functionalities are shown; among the typical, some of them emerge as of particular interest for the ALPHA Project itself:

1. In light blue on the right, the software module devoted to the handling of the IPSec connectivity protocol of the device. Such a module is of particular relevance for the support of the Femto Node transparent connection, as described in [3]. This, almost uniquely among the different ALPHA related features of the gateway, is already available in off-the-shelf devices, so will not be a subject for this document which is focused on new functionalities.
2. In light red, close to the previous block, the UPnP QoS software module; this module is, as the name clearly states, of relevance for the implementation of the UPnP Quality of Service as largely described in [4].
3. Right below the previous block, the UPnP software module is shown, that is necessary for the implementation on the device of the UPnP QoS functionalities. This, alongside with the previous, are not already available on the commercial gateway, and therefore need to be ported; the description on the proposed porting strategy can be found in section 3.2

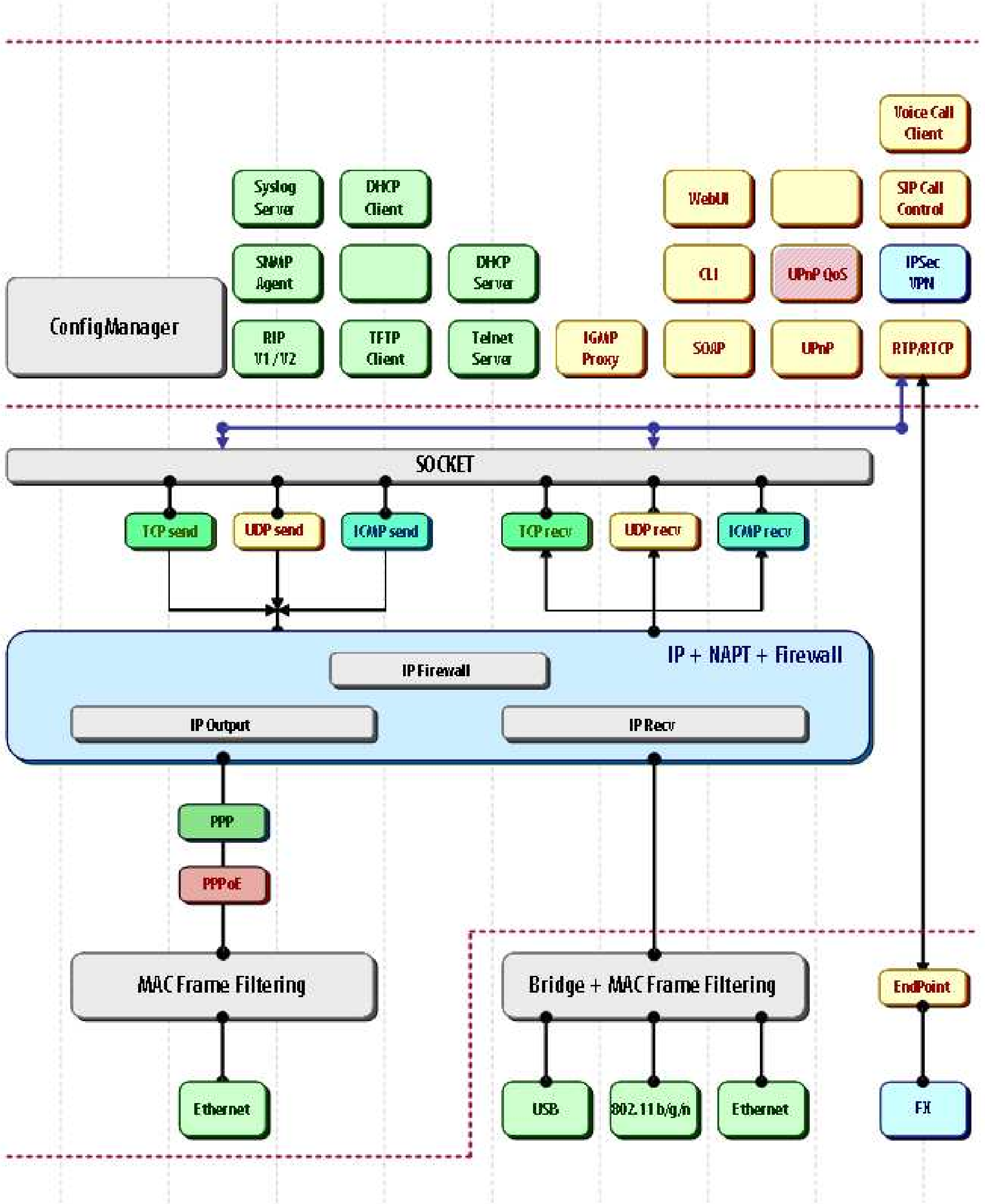

Figure 2.5 – Functional architecture of the software platform

3 Experimental results on ALPHA specific features

In the present chapter, details concerning the development and implementation of ALPHA specific features of the residential gateway are given.

3.1 POF module

As widely discussed in previous ALPHA Deliverables (for instance, [4]), one of the proposed media solutions for the Home Network connectivity is the usage of Plastic Optical Fibres (POFs); as a straightforward consequence, the integration of a POF transceiver with the Residential Gateway became mandatory.

Here below the details to reach such integration are provided.

3.1.1 Description

Basically, two main solutions were devised (see [2]), as possible choices: a "real" integration of a POF transceiver on the RG main-board[2] or the use of an external module that acts as a media converter between the electrical interface of the RG and the POF cable itself.

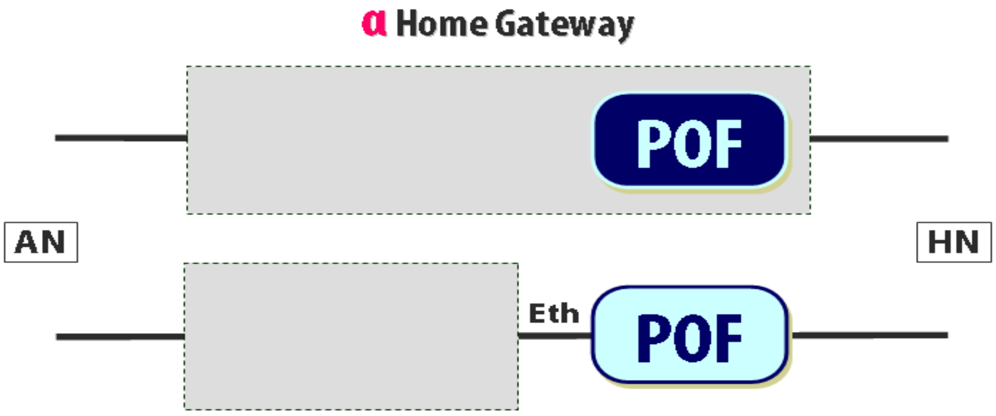

Figure 3.1 – Proposed solutions for RG-POF "integration"

The two different approaches are shown in Figure 3.1: the "integrated" solution is the upper one, while the external module is on the bottom of the picture.

The external module provides a solution that is much easier to implement, in terms of modifications on an available RG platform: it is straightforward to see that in fact no hardware modifications are required on the gateway and all the interfacing burden is placed on the external module.

However, despite the easiness of implementation, this approach shows a major inconvenience for the final user that overcomes the different advantages: in fact, such a solution requires a further piece of equipment for every POF cable that must be connected to the RG, this being especially true if the Home Network architecture is Point-to-Point (P2P).

Taking into account this last remark, the solution of choice for the ALPHA Project is the realisation of a prototype of RG that hosts the required POF transceiver directly onboard.

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[2] In this case, integration must be intended as mounting an external module as a whole on the main-board, which provides power supply to the module - and of course all the required wiring; however, the module itself must be considered as a single macro-component.

3.1.2 Partners involved

Telsey, Luceat.

3.1.3 POF module details

The lack of standardization about “Ethernet over POF” even for the 100Mbps or the 1000Mbps interfaces has left the manufacturers of POF transceivers quite free in the development process of their devices.

The main consequence is that there are already available devices from different manufacturers for 100Mbps Ethernet connections that use different electrical interfaces, digital modulation, light sources, connectors and so on. This is true also for the gigabit interfaces; in this case, the development of the transceivers is today at a “prototyping stage”, which leads to a more difficult decision about the selection of the devices that will be integrated in the RG.

As for the integration the main parameters are the electrical interface and the signalling between the transceiver and the core switch of the RG, considering the possibility to interface up to four optical ports to support the P2P approaches and the support of even 100Mbps and 1000Mbps interface with no need to redesign the board.

The transceivers for Fast Ethernet connections over POF available on the market can be classified, by signal modulation over the optical channel, in two classes:

- 100 BASE FX

  This kind of transceivers supplied by different manufacturers (Firecomms, Infineon and others) use the same electrical signal of the silica interfaces for Fast Ethernet communication, they are typically integrated in small packages and are characterized by maximum operating distances over standard numerical aperture POF ranging from 30 to 60 meters.

- MLT-3 (100 BASE TX)

  This kind of transceiver developed by Luceat shares the same electrical interface with the standard electrical Fast Ethernet ports and it is characterized by a maximum operating distance of 100m over standard POF.

From the integration point of view, the MLT-3 based transceiver seems to be the more suitable solution because it doesn't require any substantial changes to the RG board, due to the fact that all the electrical signalling needed by the transceivers (up to 4) is already available on the board itself.

However, the requirement to have a single RG board that can support even Fast Ethernet and Gigabit Ethernet interfaces is difficult to reach using MLT-3 approaches because the Gigabit interface over copper uses four twisted pairs in two directions, so it is not directly applicable to a low cost optical interface over POF. On the contrary, the FX approach is quite similar to the Gigabit interfaces developed for gigabit transmission over silica fibre, like 1000 BASE X.

The POF market shows different approaches not only about the modulation techniques but also about the connectors; this fact is primarily related to the DIY (Do It Yourself) installation that is driving the POF application in home networking.

It is possible to identify three different approaches concerning the connectors:

- Connectors adapted from Silica Fibres

  In this class we can consider many standard silica connector like SMA, ST, SC, SC-RJ, LC and others, but it is necessary to stress that only some of them has been already standardized for POF (e.g. SMA in IEC 61754-22).

- Connectors especially developed for POF

  In this class it is possible to include consider SMI (Small Media Interface, proposed in the IEEE1394 Working group), F05 and F07 (used by the Toslink systems for connecting digital audio components), MOST connectors (used in vehicle networks), V-Pin connectors (developed by Hewlett- Packard, now Avago, for industrial communications).

- Crimpless or Connectorless solutions

  The first class “Crimpless” identifies connectors already mentioned in the previous classification, but developed without the need of any crimping tool. This can be considered a step towards the DIY approach.

  The second class “Connectorless” is probably the most interesting approach in the home networking scenario; different solutions from many manufacturers like Infineon, Firecomms (Optolock^{TM}) and others, can be mentioned in this category.

There is still an open discussion on which is the best connecting solution for POF. Besides, within the ALPHA project, the partners involved in this task have agreed to avoid the use of a connectorless solution for two main reasons:

- on first place, the connector less approaches as of today have not been standardized yet
- on second hand, the prototyping stage of the Gigabit POF transceiver requires connectors and receptacle that could be easily modified within the premises of the developer, without the need for external prototyping steps, that could increase costs and development time.

In agreement with the previous considerations, within the ALPHA project, Luceat is developing a gigabit transceiver with the following characteristics:

- Electrical interface compatible with 1000 BASE X silica transceivers
- Standard SMA optical connectors (as defined in IEC 61754 part 22)
- Compatibility with lower speed signal 100 BASE FX

The last characteristic requires a core switch on the RG that is able to support the double speed option (100Mbps and 1000Mbps).

As stated before, a separate transceiver is needed for any physical POF interface that equips the RG; due to the size of POF connectors, the partners have agreed to integrate on the prototype RG board only two POF transceivers. This is the starting point to test the RG in the testbeds at least with tree and ring topologies. On a different note, it is important to point out that the differences between the commercial and the ALPHA gateway are not limited to the insertion of the transceivers, but also to the replacement of the switch module; the one that equips the commercial device is in fact not suitable to support the 1000 X modules that have been provided by Luceat.

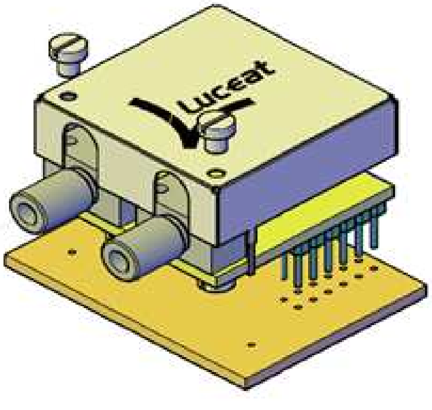

Figure 3.2 – Pluggable transceiver

The POF transceivers have been integrated on different PCBs, in a "plugin" style in which the transceiver boards are placed with a soldering connector to the RG boards - see Figure 3.2; in such a way the transceivers could be upgraded to test different configurations and optical properties of the transceiver itself as already noted in [5], with no need to redesign the RG board.

As can be noted from the previous sketch the transceiver doesn't have a standard form factor like SFF, SFP or 1x9; this is due to the fact that the pin out and dimensions of the transceiver have been agreed during the development of the transceiver itself, trying to reduce the dimensions of the device keeping them flexible for future optic and electronic changes, as long as the prototyping phase is still in progress.

The overall dimensions and electrical interfacing between RG and POF transceiver has been agreed between partners in June 2009; the dimensions are shown in Figure 3.3.

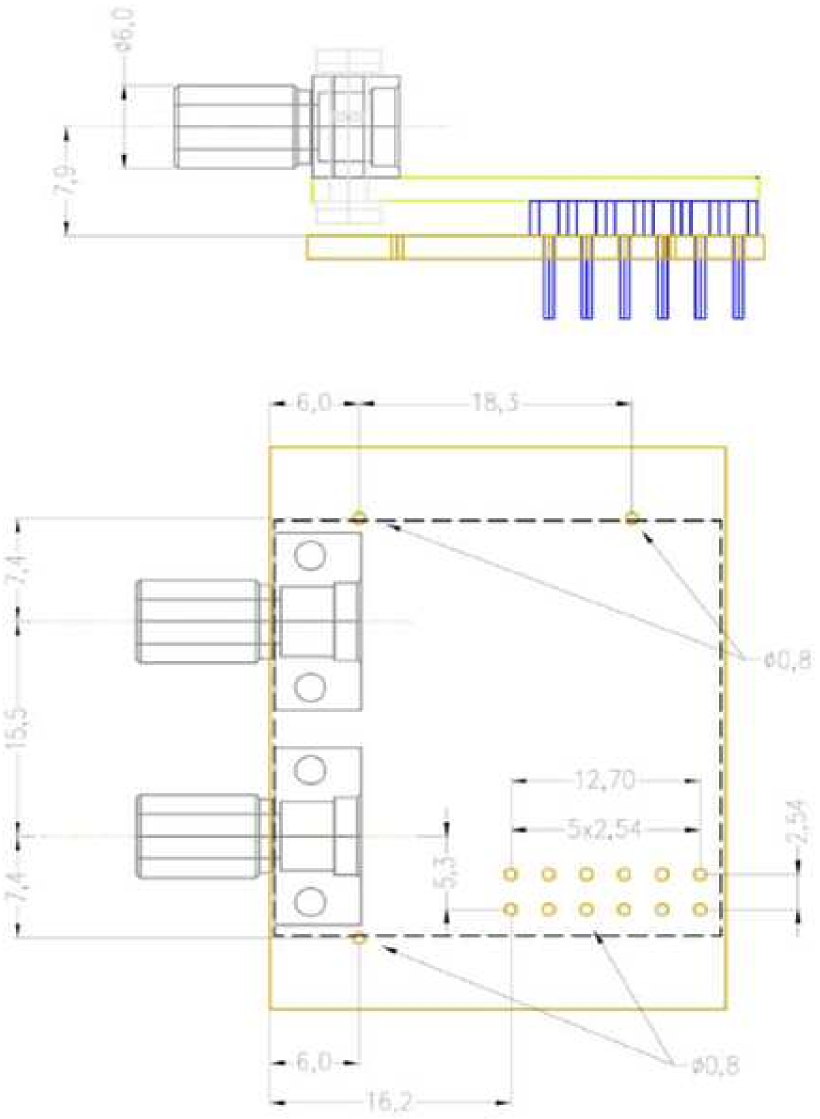

Figure 3.3 – Mechanical dimension (all dimensions given in millimeters)

As can be form the picture, the overall size of the transceiver is imposed by the SMA connectors and the soldering connector to the PCB of the RG. The placement of the electrical interface connectors is due to the envisioned possibility to mount the transceiver not only in a horizontal way but even in vertical, limiting the overall size of PCB area required on the RG board, but obviously increasing the height of the RG enclosures; the vertical mounting of the POF module is sketched in Figure 3.4.

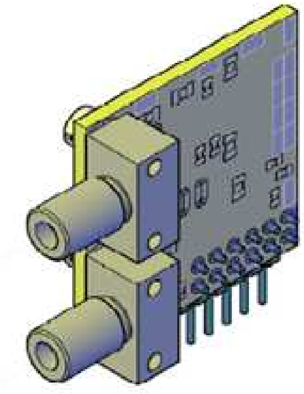

Figure 3.4 – POF transceiver Vertical Mounting

The pin out is strictly related to the properties that the transceiver must satisfy; such properties can be collected from [5], and are reported in the following for simplicity:

- ***"Cost Effective Solution"***
  All the solutions implied in the transceiver must be derived from *off-the-shelf* electronics or optics, with no need to develop ASIC or special coupling optics.

- ***1000 BASE X and 100 BASE FX Compatibility***
  Strictly related with the first requirement, these signalizations are the only applicable choice to apply to the transceiver not only in laboratory environment as a standalone device, but it could be simply integrated with third party technologies with no need to design an ad hoc PHY (Physical layer from and ISO/OSI stack point of view).

- **Encoded data Stream**
  Encoded stream normally used in optical communication to ensure a constant overall optical power transmitted, avoiding long sequences of 1s or 0s to ensure an immunity to low speed variations due to AC coupling even in the transmitting or receiving side. This encoding should be 4B5B for fast Ethernet (100 BASE FX) or 8B10B for gigabit ethernet (1000 BASE X), as stated by the IEEE 802.3 documents.

- ***1,25 Gbps Maximum Raw Data Rate***
  The encoding proposed has an overhead of 25%. In fast ethernet communication each 4 bits of data are transmitted as 5bits and in gigabit communication each 8 bits of data are encoded in 10bits.
- ***Target BER < 10-12***
  Bit Error Rate (BER) requirement in ethernet fibre communications, ensuring this target error rate doesn't require any error correction techniques like FEC (Forward Error Correction) or other similar approaches.

- ***Distances close to 50m***
  This distance is the minimum target to be reached for POF communications in in-building environments as specified in the Annex of ALPHA project.

All this functions and requirement have been reflected in the RG board interface to the POF transceiver that is explained in the next section.

3.1.4 Architectural details of the new RG board

The interface between RG and POF transceiver has been made using a standard 6 x 2 2.54mm PTH (Place Through Hole) connector; the choice of a PTH over an SMD (Surface Mounting Device) approach is related both to the "low cost" requirement and to ensure an overall mechanical stability of the joint device (RG and POF modules).

In addition, in order to respect the electromagnetic requirement for in building devices (e.g. EN55022 and EN55024), an RF shield has been added with three pins that need to be soldered to the RG Board. The RF shield has been integrated within the transceiver keeping in mind that the RG includes at least one radio device, like a Wi-Fi interface.

Furthermore, the POF transceiver has been developed to respect the emission limit of the EN55022 and to avoid interferences not only as requested by the residential normative like EN55024 but even for Industrial and harsh environments (e.g. EN61000-4); this allows a safe placement of the transceiver within the RG board.

The pin numbering of the interface is detailed in Figure 3.5:

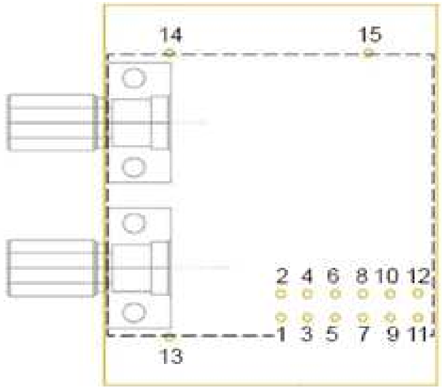

Figure 3.5 – Pin out numbering

The pins functionalities can be summarized as in the next table:

Pin	***Symbol***	***Description***	***Direction***
1	IN_{HI}	Input signal high	IN
2	IN_{LOW}	Input signal low	IN
3	GND_{TX}	Transmitter Ground	POWER
4	FLT	Transmitter Fault indicator	OUT
5	V_{TX}	Transmitter +3.3V	POWER
6	EN	Transceiver Enable	IN
7	GND_{RX}	Receiver Ground	POWER
8	OUT_{LOW}	Output signal low	OUT
9	V_{RX2}	Receiver +3.3V	POWER
10	OUT_{HI}	Output signal high	OUT
11	LOS	Loss of Sync	OUT
12	V_{RX1}	Receiver +5V	POWER

13	SHL	RF shield	SHL
14	SHL	RF shield	SHL
15	SHL	RF shield	SHL

Table 1 - Pin Out description and Symbols

The signals required by the Ethernet PHY are the in-coming differential signal (IN_{HI} , IN_{LOW}) and the out-coming signal (OUT_{HI} , OUT_{LOW}).

In addition to these signals and in completion of the requirements listed in section 3.1.3, during the development process of the POF gigabit transceiver some other features and signals have been added:

- ***Built-in LOS (loss of sync)***
  The transceiver needs to signal the MAC (Medium Access Control) device the absence of the fibre or a malfunctioning connection due to improper cabling or connectorization. This signal is typically required to establish a correct fibre link also in silica fibre connections. In standard MMF and SMF connection this signal is only related on the optical power received; in the POF scenario is related not only to the received power but also to the bandwidth of the overall link and the correct equalization of the incoming signal.

- ***Enable signal***
  The transceiver may be put by the upper layers of the ISO/OSI stack in a low power mode in which the transmitter is totally powered off. This “low power mode” needs to be activated by the RG or by the device that embeds the upper layer stacks. It is possible to include a simpler low power functionality even in the transceiver connecting the LOS (Loss Of Sync) and EN (ENable) together: in this way, the transmitter is disabled when there is no incoming signal in the receiving side.

- ***Flexible electrical Interface***
  The received and transmitted signal are internally terminated and AC coupled, in this way the interfacing with other devices is simple and doesn't require any external components, the electrical levels of the transmit and receive pairs are compatible with LVDS (Low Voltage Differential Signaling), but could be easily connected to CML (Current Mode Logic) or ECL (Emitter Coupled Logic).

- ***Transmitter Fault***
  Any malfunctioning on the receiving side could be locally exploited by the LOS signal, but the transmitter fault without a specific signal is difficult to be exploited.
  This kind of malfunctioning is typically shown on the remote receiving side that could advise the local transmitter that something is not working properly.
  This is the reason to integrate a transmitter fault signalization that, depending on the source used, may exploit an unexpected thermal behavior or a shift of the optical characteristics of the light source and driver module.

All the functionalities introduced in this paragraph have been detailed in [5].

As can be noted from the pin description in Table 1, the Receiving and Transmitting side have separate ground references[3] to avoid the possible cross-talk between the incoming and outgoing signals. The power supplied requires two different voltages: +3.3V and +5V, the transceiver works well even with only 3.3V but powering the receiving AGC (Automatic Gain Control) block with 5V improves the noise performances that are required to reach the 50m POF distances with comfortable power margin.

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[3] this respect the layout of the PCBs in which the two sides have different ground planes

The power consumption of the device is close to 1W in normal operating mode, with bidirectional transmission over 50m of POF. This consumption could be reduced as low as 0,2W disabling the transmitting side and reducing the power of the AGC block.

Concerning the adaption of the existing RG platform, the following figures will help in explain the required modifications.

In Figure 3.6 is shown the schematic of the commercially available RG used in the ALPHA project; making a comparison with Figure 2.3 it is possible to identify the correspondences:

- in this RG model, the Main Processor and the Switch shown in Figure 2.3 are integrated in a single component, the Network Processor which is shown in the middle of the picture
- in the lower part of the picture, the SLIC/SLAC interfaces are shown, corresponding to the FXS1 and FXS2 interfaces, connected to a couple of RJ11 electrical ports for the connection of up to 2 VoIP telephones
- on the left side of the picture, the 2 USB hosts are shown, directly provided by the Network Processor
- on the upper right side, the Wi-Fi section of the device is shown, comprising the Wi-Fi baseband processor, the Transmitter amplifier, the Receiver transceiver, and the 3 antennas of the device (which implements the IEEE 802.11n standard).

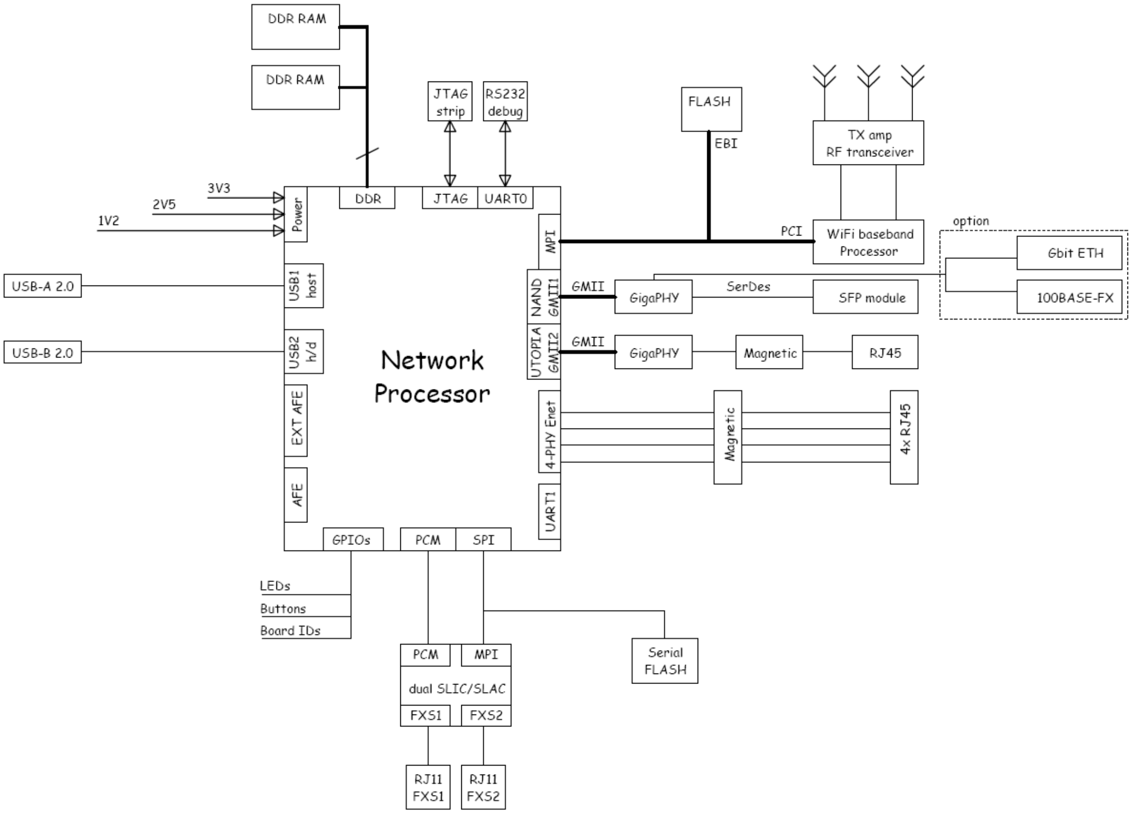

Figure 3.6 – Commercially available RG platform

As anticipated, however, all this components are unaffected in the Gateway designed for the ALPHA Project; in fact, comparing Figure 3.6 and Figure 3.7, where the modified schematic is shown, it is immediate to spot that the aforementioned sections of the device are exactly the same.

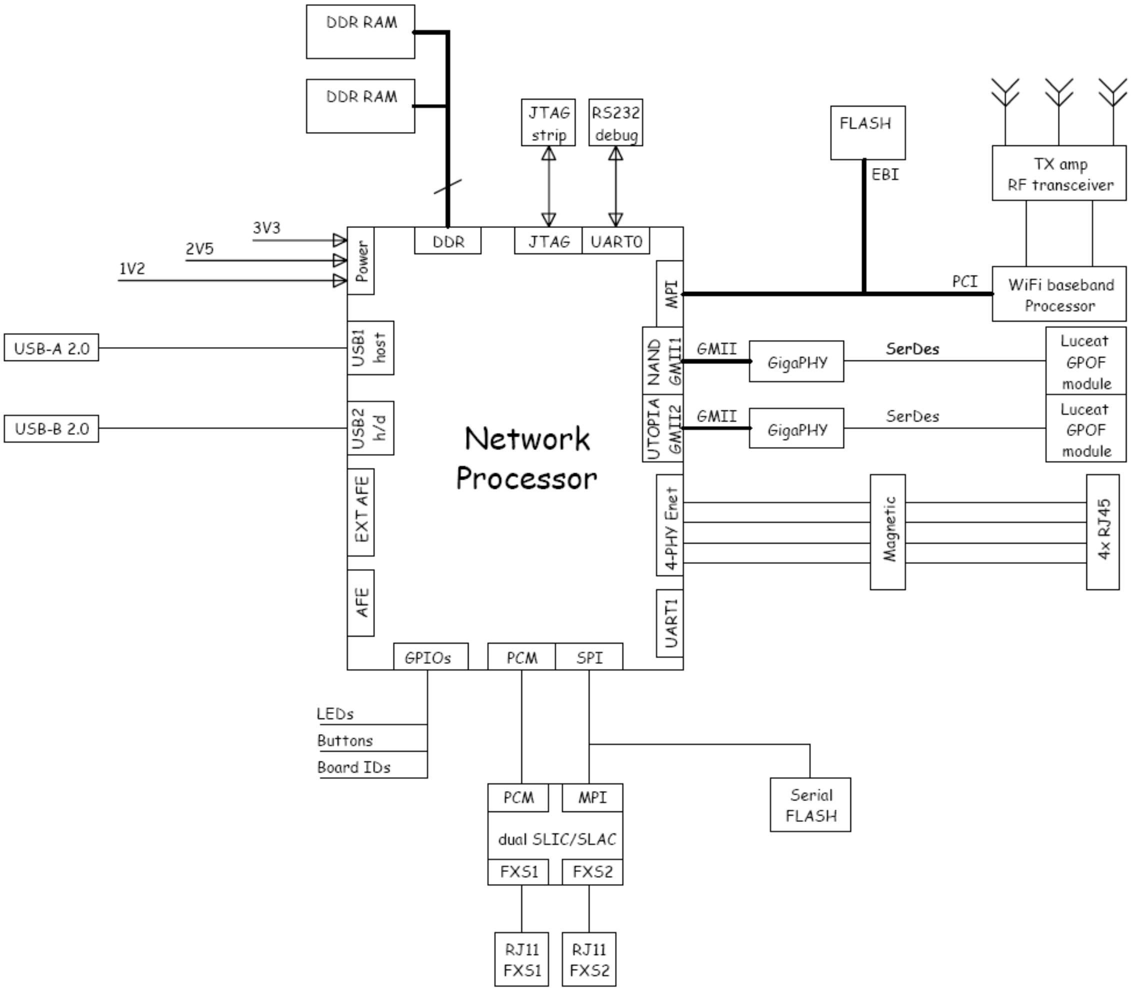

Figure 3.7 – ALPHA-modified RG platform

The functional area of the device where the major changes took place is the Uplink/LAN section, which is shown in the middle/lower part of Figure 3.6 and Figure 3.7; such a portion of the schematic had been detailed in the two following pictures, Figure 3.8 and Figure 3.9, which are simply a zoomed version of the previous ones.

Looking at Figure 3.8, it is possible to identify two port blocks:

- in the lower part of the right side, the 4 Fast Ethernet LAN ports are shown, connected almost directly to the Network Processor
- right above the LAN ports, the Giga ports are shown: the upper one is terminated on an SFP module for the fibre uplink, while the second one is terminated via an RJ45 connector (that is currently unused on the original device). The Giga ports are not directly connected to the device, but require an intermediate component acting as an interface, here indicated simply as GigaPHY. Note that the two GigaPHY blocks in this schematic are not the same component - even if that is not made evident in the picture - as long the required interfacing toward the end connector are different.

Looking instead at Figure 3.9, it is possible to identify similar blocks, however with different functionalities:

- in the lower part of the right side, the same block of 4 Fast Ethernet ports is present; however, in this case, 3 of the 4 ports are dedicated to the LAN, while the 4th one is software segregated form the others and dedicated to the WAN uplink. Therefore the ALPHA residential gateway will have a Fast Ethernet uplink.

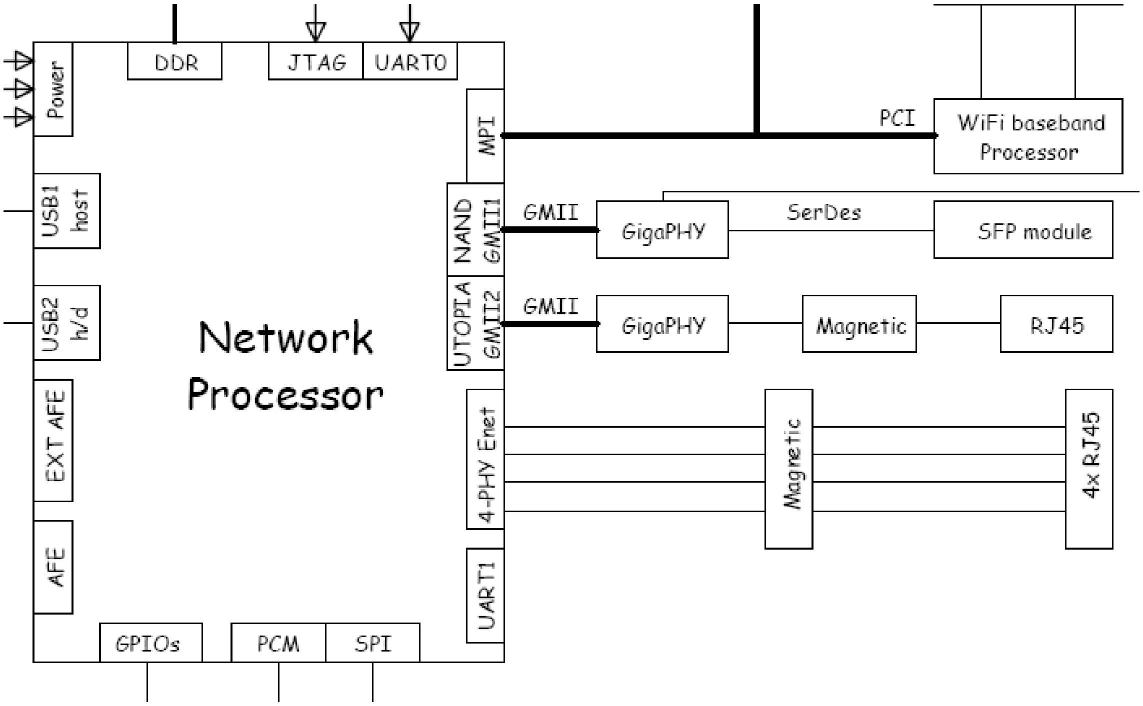

Figure 3.8 – Commercially available RG platform; detail

- in the upper part, the 2 Giga ports are shown; in this case, the interfaces on the Network Processor are (GMII1 and GMII2) are connected to a GigaPHY block which is the same for both the interfaces and that provides connectivity to the POF modules provided by Luceat profusely described in section 3.1.3.

As can be seen form the pictures, therefore, the adaptation of an existing RG hardware platform was extremely limited, in according to the will express in the Technical Annex of using only available devices.

Concerning the last sentence, it is worth to note that the proposed solution was not the only one evaluated; in fact, a different architecture that required a Giga Switch external to the Network Processor was also take into account. Such architecture would have provided interfaces for up to 4 external POF modules, leaving intact the uplink and LAN part shown in Figure 3.8.

However, such a modification, would have required a deep redesign of the RG board to properly include the external switch, therefore was discarded during the project analysis.

As a consequence, having two Giga interfaces available on the Network Processor set the limit on the number of POF modules that the RG is capable on manage to 2. This limitation is, on the other hand, made almost irrelevant by the sheer physical size of the POF modules; as stated in the previous section, in fact, the dimension of the transceivers make it impossible to host more than 2 of them on the RG platform adopted as the base for the ALPHA device.

To conclude the description of the modification on the RG board, two last remarks:

- the powering to the POF module, not shown in the pictures, is provided - as one should expect - by the powering section of the RG

- the pins of the module that are not directly involved with data transmission (see Table 1 for the complete list) are connected to the GPIOs ports of the Network Processor; these connections are not shown in the pictures only for simplicity.

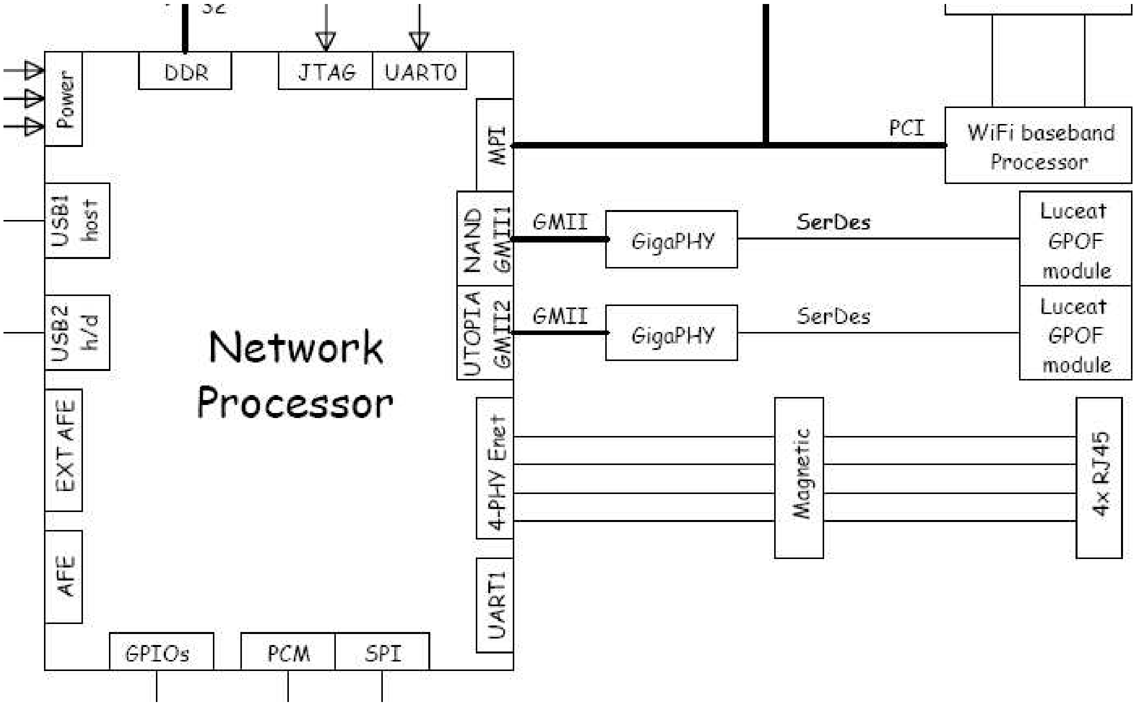

Figure 3.9 – ALPHA-modified RG platform; detail

3.1.5 Experimental characterisation of the new RG functionality

As stated in [5] and in the previous sections the POF modules integrated within the RG Board are devices still in the debugging stage of their development in the ALPHA project. Different versions of the transceiver have been developed and tested: all these devices share the same hardware interfaces and functionalities already described and therefore they could be integrated on the RG without need of further modifications of the RG board.

The POF transceiver is a Layer 1 (L1) device, a pure physical module that can be fully characterized from a “system” point of view using a BER (Bit Error Rate) tester; this measurement gives the probability to have an error in the detection of a received bit within a programmed random data stream and in a specified amount of time, without the need to consider other parameters like network issues or network interfaces loading.

In [5] the BER measurements are reported at different length of fiber that has been obtained with Luceat POF gigabit transceivers.

It is relevant to note that the BER results obtained over the POF module are quite different from the typical behavior of BER measurement of silica fiber connections, which are typically related only to the incoming signal power level; in fact, in a typical BER characterization of a high speed system, as the power at the receiver is decreased, the Signal-to-Noise Ratio (SNR) is reduced and therefore the probability of a bit being incorrectly detected increases.

This remains true even for the POF case; however, the BER measurement is also affected in a not negligible way by the bandwidth of the fiber.

Taking this last remark into account, it is straightforward to conclude that the BER measurements in the POF case cannot be conducted with optical attenuators to simulate different POF lengths but there is a need to use real fibers.

On the other hand, it must be considered that the bandwidth limitation of the fiber is the primary cause of jitter increasing, and such increasing is reflected in the BER performances; however, this effect is limited and partially solved by the use of the Channel Equalizer (see [5] for details).

The Channel Equalizer controls also the LOS (Loss of Sync) signal. The underlying algorithm goas as follows:

- as stated before, lowering the bandwidth of the overall channel increases the output signal jitter
- the jitter value is monitored by the Channel Equalizer
- when the jitter exceeds a predetermined level, the Channel Equalizer asserts the LOS signal and the transmission is disabled.

In such a way, if the proper jitter level is set in the Channel Equalizer module, the transceiver could alert the network processor that something is going wrong in the physical layer prior to note a BER increase and the consequent malfunctioning of the upper network layers.

Due to the developing stage of the POF transceiver the LOS functionality, as agreed between partners, has been activated to limit the functionality of the first version of the POF module integrated on the RG board only to connections distances lower than 10m of standard numerical aperture POF; with the LOS signal operating in such a fashion, the testing of the POF transceivers shows a $BER < 10^{-12}$ with fiber distances up to 10-15m; if the POF length is increased, even if the received optical power is enough to be detected by the receiver chain, the LOS signal is asserted and the transmitter goes to low power mode.

This limitation has been introduced only to correctly characterize and test the interaction between the gateway and the POF module and should be removed in the next months with the upcoming version 0.3 of the POF transceiver that solves the noise floor problems already detailed in [5].

In the following pictures, an overview of the almost final device is shown.

In Figure 3.10 the POF transceivers are shown (see Figure 3.3 for a comparison and [5] for further details):

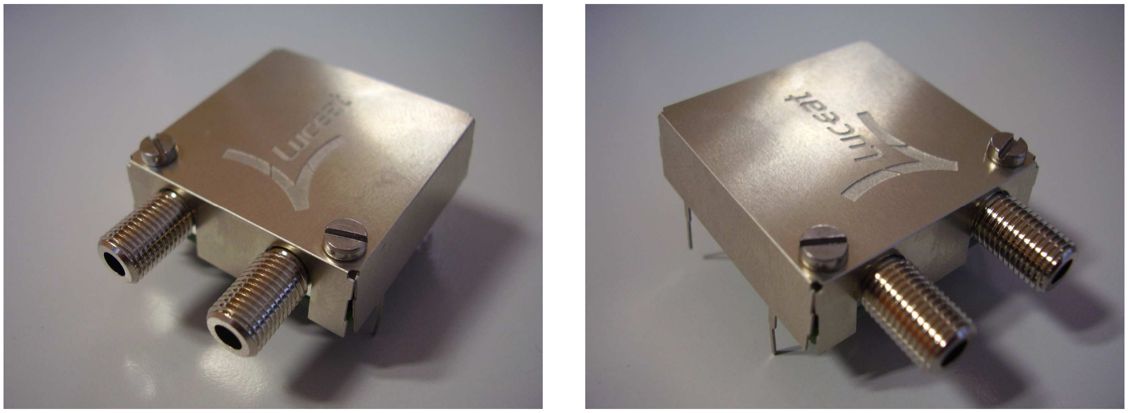

Figure 3.10 – 1Gbps POF transceivers provided by Luceat

In Figure 3.11 the Residential Gateway board is shown as developed by Telsey[4]; in detail, in the picture it is possible to spot:

- the Network Processor, in the middle of the board
- the 4 copper Ethernet ports (in black), devoted to LAN and WAN connectivity
- the 2 VoIP ports (in gray)
- the 2 USB host ports, in the upper corner of the device
- the 3 antennas of the Wi-Fi compartment on the cut corner of the board

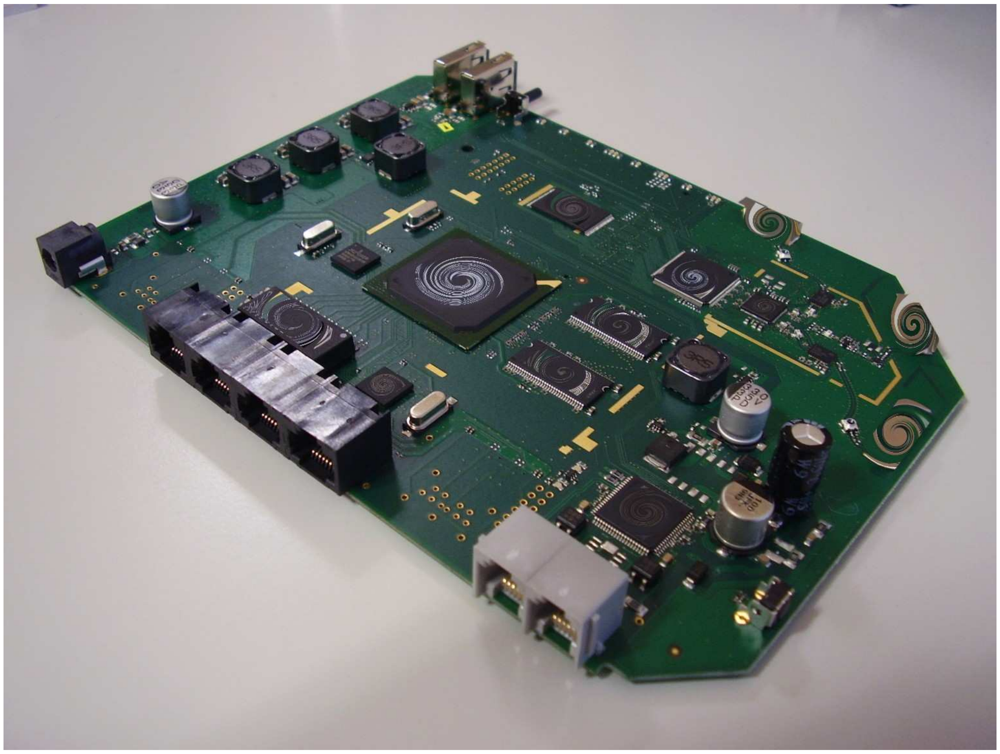

Figure 3.11 – ALPHA Residential Gateway board provided by Telsey

In Figure 3.12 and Figure 3.13 the final version of the ALPHA Residential Gateway is shown; as can be seen, the final prototype has 2 GigaPOF transceivers. From the pictures it is also possible to note the size of the POF transceiver with respect to the rest of the board; as stated before, the maximum number of transceivers was limited both by the HW platform of choice and also by the sheer space occupation of the POF modules. To overcome such limitations, a large board redesign will be required.

In Figure 3.14, finally, the almost final device is shown: the board is mounted in its external shell, with just the back panel missing.

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[4] some of the board details have been unfocused on purpose, in this and in the following pictures

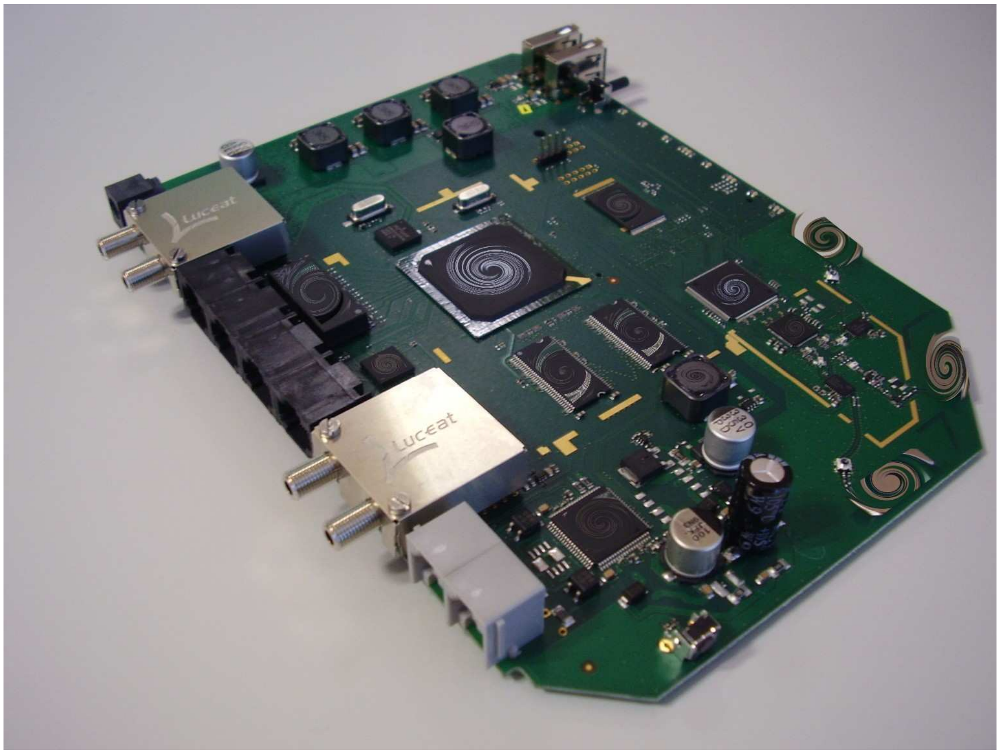

Figure 3.12 – ALPHA Residential Gateway board (1)

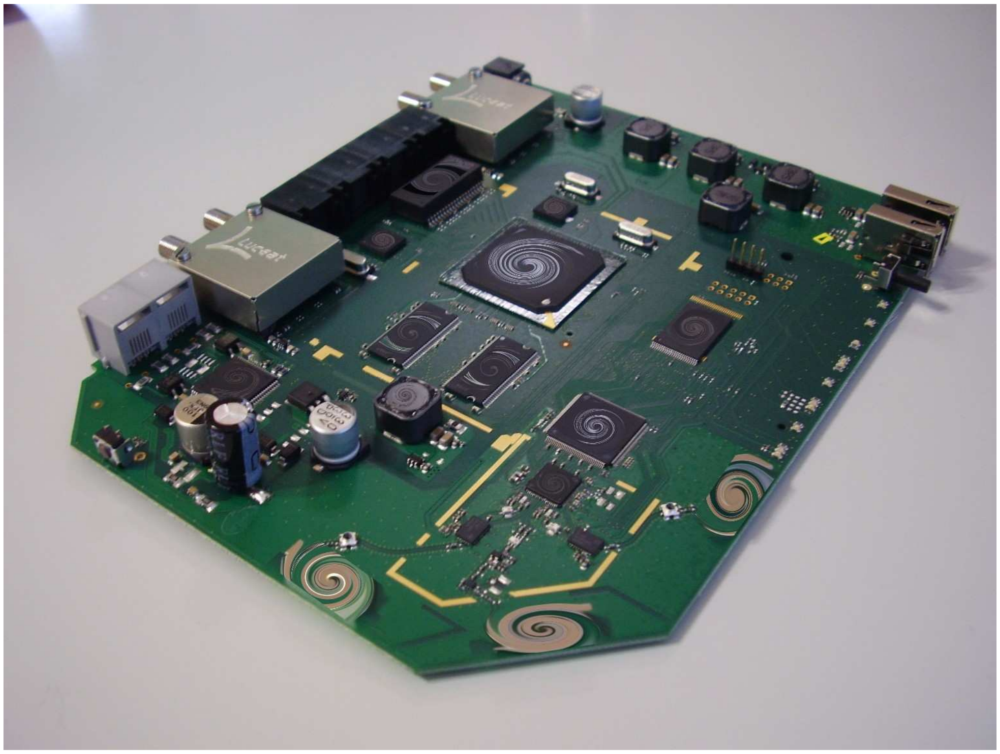

Figure 3.13 – ALPHA Residential Gateway board (2)

Figure 3.14 – ALPHA Residential Gateway with external shell

The complete results about the experimental activities concerning the new RG functionalities with the final version of Luceat transceivers, that are currently in development and that will extend the link length up to 50m of POF, will be reported in the D5.5 as part of the field trials activities within Telsey and Luceat premises. Further details can be found in section 4.2.

3.2 UPnP QoS

A detailed description of UPnP QoS can be found in [6], [7] and is outside the scope of this document; in the following, however, the key elements of UPnP QoS are briefly overviewed in order to identify the requirements for the implementation on the RG.

3.2.1 Description

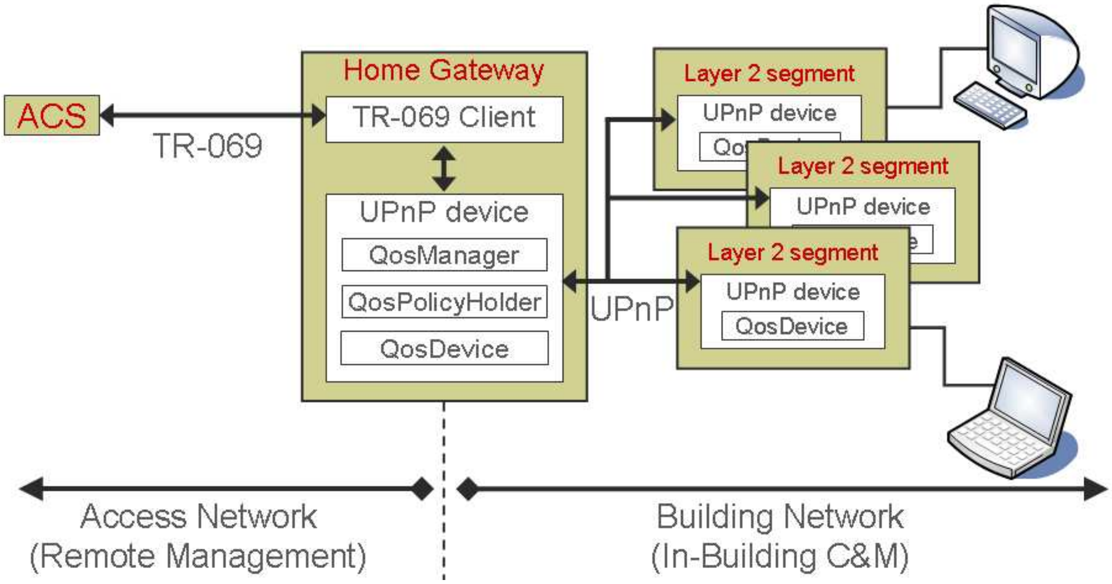

Figure 3.15 – Overview on UPnP QOS

In Figure 3.15 is depicted a typical configuration for an UPnP QoS solution; such a scheme is also to be intended as a minimal UPnP QoS setup inside the ALPHA Project. The picture highlights all the relevant elements of the QoS architecture:

- The ACS, communicating with the Home Gateway (HG) via the TR-069 protocol (CPE-WAN Management Protocol, CWMP) for remote management and configuration of the end devices.
- The Home Gateway itself.
- The LAN side end devices, connected to the HG.

From the picture it is straightforward to identify the requirements that the HG must satisfy in order to fully[5] support the UPnP QoS functionalities:

- Implement a TR-069 client, to communicate with the ACS
- Implement the 3 services defined by the UPnP QoS architecture ([7]):
  - QosPolicyHolder: repository of rules for QoS policies
  - QosManager: allows Control Point (CP) to setup/release/update QoS for traffic streams
  - QosDevice: manages resources of a QoS-capable device

Several solutions can be devised in order to fulfil such requirements, each one of them introduces a certain amount of complexity on the RG. These solutions were analysed in detail in [2], in order to define the solution of choice for the ALPHA Project; in the following the guidelines for such a solution are briefly reported.

3.2.2 Partners involved

IBBT, Telsey

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[5] in the following, it will be shown how such requirements could be relaxed

3.2.3 Implementation on the RG: different approaches

The architectural solution shown in Figure 3.15 was completely developed by IBBT emulating the behaviour of the Home Gateway via a PC on which the UPnP QoS services were coded in Java. Goal of the activity carried on during the project was the insertion of a real RG in the above scheme.

As anticipated, several solution were evaluated to achieve such integration: in Figure 3.16 the simplest (with respect to the RG) one is shown: the UPnP QoS services are implemented in a different/external device, indicated in the picture as “IBBT Home Server” and corresponding to the Home Gateway in Figure 3.15, while the RG simply forwards the TR-069 connection from the ACS down to the Home server.

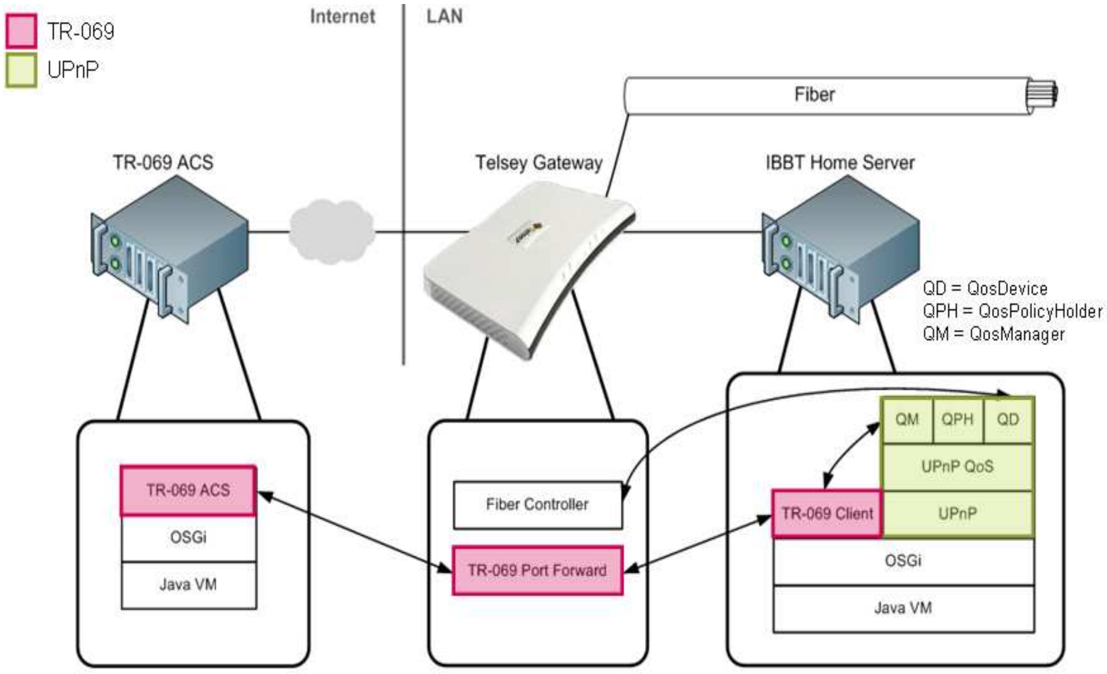


Figure 3.16 – UPnP QoS proposed solution: no UPnP software on the RG

As can be seen from the picture, all the UPnP QoS services (QM, QD, QPH) are located on the Home Server; such server interacts with the RG as long as the RG itself is demanded to provide the low level mechanism to implement the UPnP QoS functionalities and that concern mainly the queuing mechanisms of the packets on the medium (fibre and fibre controller in the picture).

So, the Telsey Gateway in the picture acts as an interface for the IBBT Home Server towards both the Access Network and the End Devices located inside the Home Network.

Such a solution cast very little requirements on the RG but, on the contrary, requires the presence of an external device, the Home Server.

In order to remove the need of an external device, a solution of choice for the scope of the ALPHA Project has been identified and depicted in Figure 3.17. As can be immediately spotted observing the picture, there is no longer the Home Server in the HN side; the reason for this is that all the UPnP QoS related functionalities are ported on the RG.

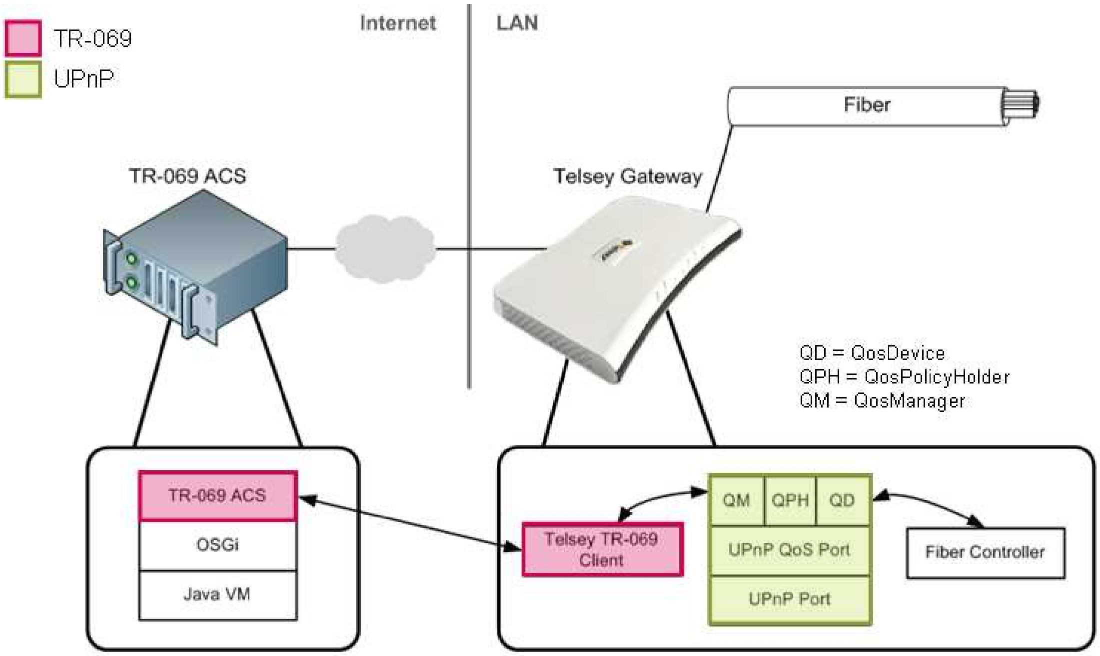


Figure 3.17 – UPnP QOS proposed solution: complete porting on the RG of the UPnP QOS functionalities

This solution, as could be expected, cast the most severe requirements on the RG, but allows the HN (and therefore the user) to avoid including an external, additional piece of equipment (the Home Server); to summarize, this approach requires that:

- The TR-069 client is hosted on the RG
- The UPnP stack, UPnP QoS stack, and the QM, QPH, QD Services are hosted on the RG
- The L2 queuing mechanisms (the "Fibre controller") are hosted on the RG.

3.2.4 UPnP QoS development guidelines

In the previous section, the solution of choice was briefly described; the approach, as remarked, requires that all the UPnP QoS functionalities are ported from the IBBT Home Server to the Telsey Gateway. Such an operation cannot be performed straightforwardly, as long as the IBBT Home Server is based on the Java/OSGi environment that cannot be ported directly on the RG due to the limited computational power of the latter; therefore a porting of the UPnP QoS implementation from Java to C is required.

As an intermediate step in the evolution that goes from the situation depicted in Figure 3.15 (and Figure 3.16) to the desired solution of Figure 3.17, is depicted in Figure 3.18. In such a scenario, which relies on both a TR-069 client and a subset of UPnP capabilities located on the RG, the following must be implemented:

- the TR-069 client must be capable of triggering the QoS Manager on the IBBT Home Server
- the QoS Device is implemented directly on the RG
- the L2 queuing mechanisms are implemented directly on the RG

In this scenario the Home Server is still present, but it does not implement all the UPnP QoS services, as long as the QoS Device is now implemented directly on the RG; the need for this implementation is the reason behind the a porting of minimum subset of UPnP and UPnP QoS capabilities on the residential gateway, as can be clearly seen from Figure 3.18.

This intermediate step can be considered as an “hybrid solution”, due to the fact that part of the required components are directly located on the RG, while a part of them is still hosted on the Home Server.

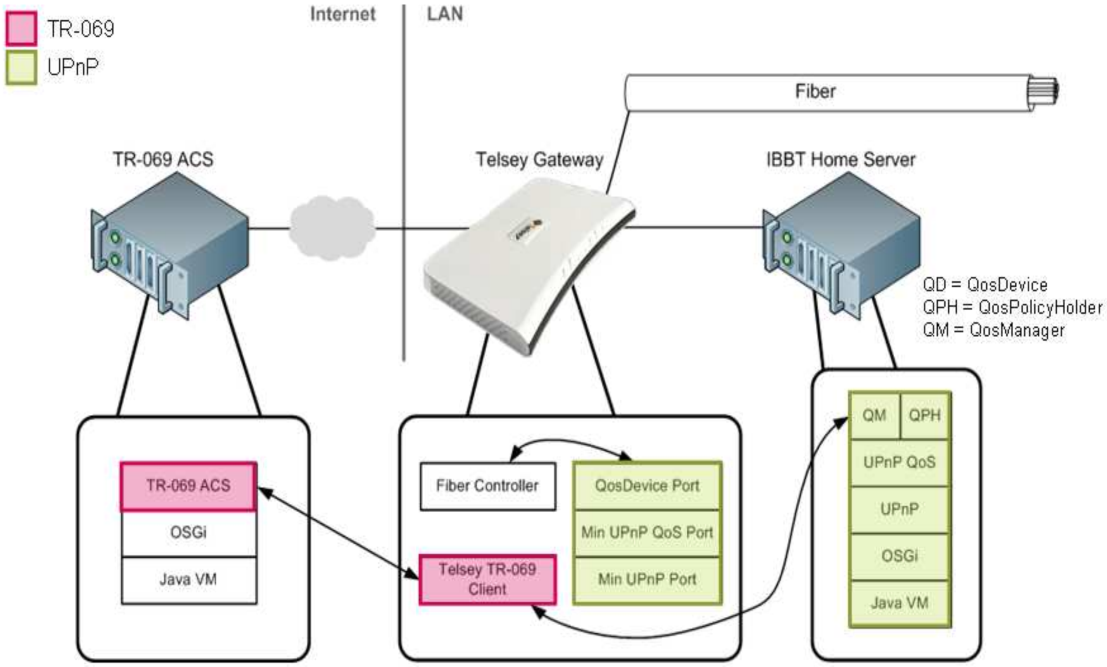
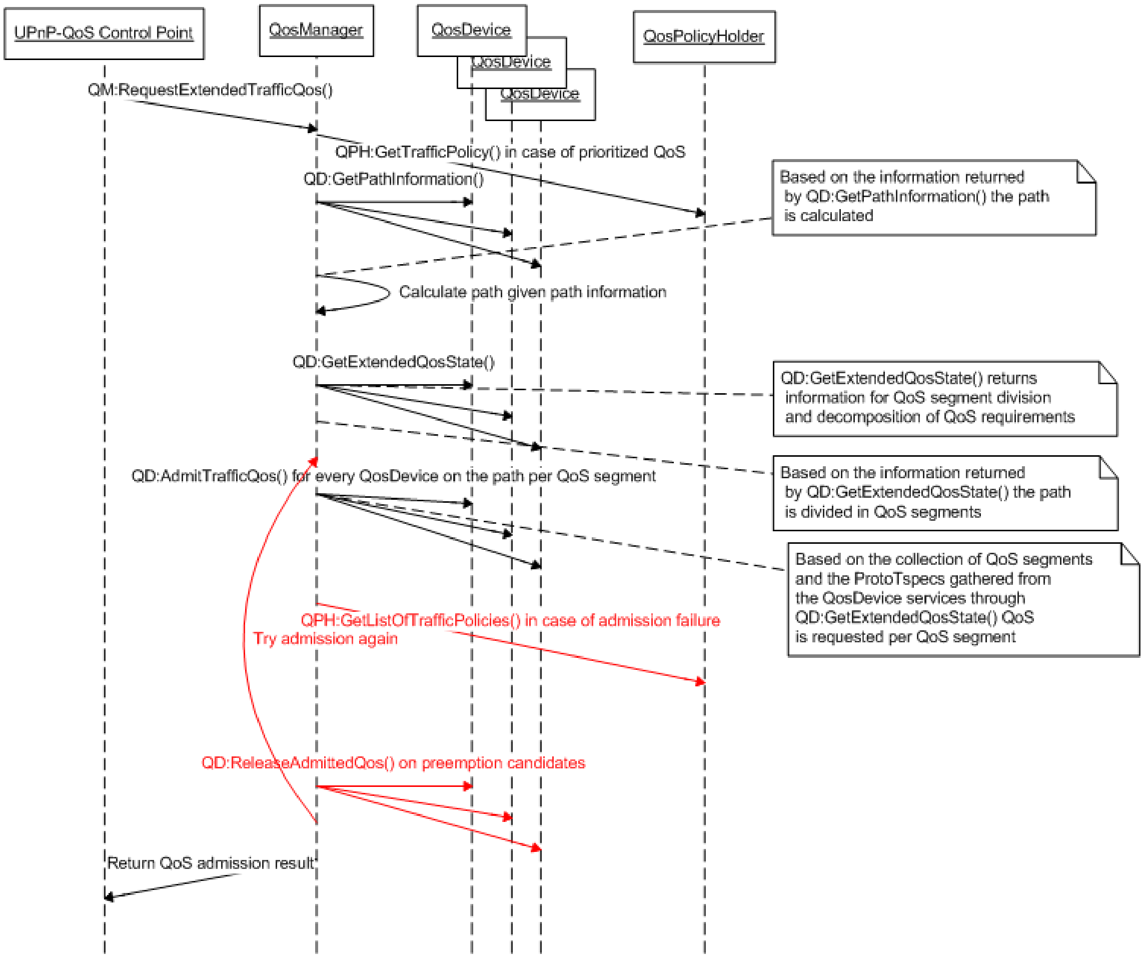


Figure 3.18 – UPnP QOS proposed solution: partial porting of UPnP services on the RG



Based on the information returned by QD:GetPathInformation() the path is calculated

QD:GetExtendedQosState() returns information for QoS segment division and decomposition of QoS requirements

Based on the information returned by QD:GetExtendedQosState() the path is divided in QoS segments

Based on the collection of QoS segments and the ProtoTspecs gathered from the QosDevice services through QD:GetExtendedQosState() QoS is requested per QoS segment

Figure 3.19 – Diagram of QoS request with optional contention resolution (preemption)

Having defined the first step of the porting as the implementation of the functionalities of a QosDevice on the RG, it is therefore necessary to identify the actions that are required for such a porting.

In Figure 3.19 is shown the diagram illustrating the setup of UPnP QoS (including also the pre-emption mechanism); among partners, the necessary subset of actions that is sufficient to realise the QosDevice on the RG had been identified, and is reported in the following:

- QD:SetPreferredQph() has to be implemented in order to retrieve the PreferredQPHId, which is the parameter that identifies the QosPolicyHolder of choice of the QosDevice; this step is not shown in Figure 3.19.
- QD:GetPathInformation() is absolutely necessary for QosManager to be able to calculate the path on which the QosDevice is inserted
- QD:GetExtendedQosState() has to be implemented in order to retrieve information concerning the network interfaces of the device including the QosSegmentId, which is the parameter that identifies the QosSegment(s) the QosDevice belongs to.
- QD:UpdateAdmittedQos() isn't absolutely necessary, as long as this action is not used by the QosManager to change parameters of an already established QoS service;
- on the contrary, QD:AdmitTrafficQos() is mandatory as long as this action is used to establish such service.

- QD:ReleaseAdmittedQos() should be implemented to be able to release a previously admitted QoS request

3.2.5 QosDevice and L2 queueing mechanism implementation details

As stated in [7], the UPnP QoS specifications does not indicate any detail on the low level implementation of the specified actions; this means that the implementation of the QoS reservation mechanism is technology specific.

While this approach does not provide indications or suggestion on how such implementation has to be done, at the same time leaves some degrees of freedom in the development of the UPnP QoS services; and such freedom is a key factor when the development is made on an already existing device, such the ALPHA gateway, and not on a device specifically designed to host the UPnP functionalities.

Considering the actual implementation of the new functionalities for the ALPHA RG, the QD has been developed in C language and is based on libupnp (the Portable SDK for UPnP device), an open source project available under BSD license. This is the most efficient solution for embedded systems with limited memory and power processing such as the available RG, but it is fine also for Linux PC and other systems with different architectures and/or OSs.

The implementation is not yet fully compliant to UPnP QosDevice v3 specifications: it includes QD required actions as reported in the previous section (GetExtendedQosState, GetPathInformation, AdmitTrafficQos, ReleaseAdmittedQos) and a partial implementation of UpdateAdmittedQos.

The RG platform includes a dedicated chip to switch LAN-to-LAN traffic at high rate, but with limited QoS capabilities: no bandwidth reservation is available, just queueing mechanisms. Therefore Prioritized QoS is supported while Parametrized QoS is not, and QD:UpdateAdmittedQos action is quite useless.

Considering the Ethernet switch, up to 4 output queues can be configured on each of the LAN ports of the RG, and packets can be classified based on IP TOS value and/or priority value of 802.1Q tag. Packets are classified and queued after switching decision and before transmission. Queues are scheduled with static priority: packets in a queue are eligible for transmission only if there are no packets waiting in other queues with higher priority. Classification decisions are configurable (e.g. to queue packets with TOS value 63 to first, highest priority, queue).

Due to these HW platform limitations, the QD L2-specific current implementation in the RG is quite poor: upon receiving an AdmitTrafficQos request, the QD configures the internal switch chip to enable QoS support and to give priority to traffic identified by TOS as specified by TrafficImportanceNumber mapping. When all established TrafficQoS requests are released, the internal switch chip is configured back to default mode (no QoS support).

To summarize, the QoS reservation mechanism of the QosDevice works as follows:

- the RG Switch is capable of handling up to 4 priority queues per LAN port, with decreasing value of priority from queue 1 down to queue 4
- the RG can assign each packet to a specific queue accordingly to the tagging of the packet

3.2.6 Experimental characterisation of the new RG functionality

In order to develop the UPnP QoS functionalities in the fashion described in the previous sections and to perform the first experimental testing of the new residential gateway features, a minimal test system was set up in Telsey labs; a schematic of the setup is shown in Figure 3.20:

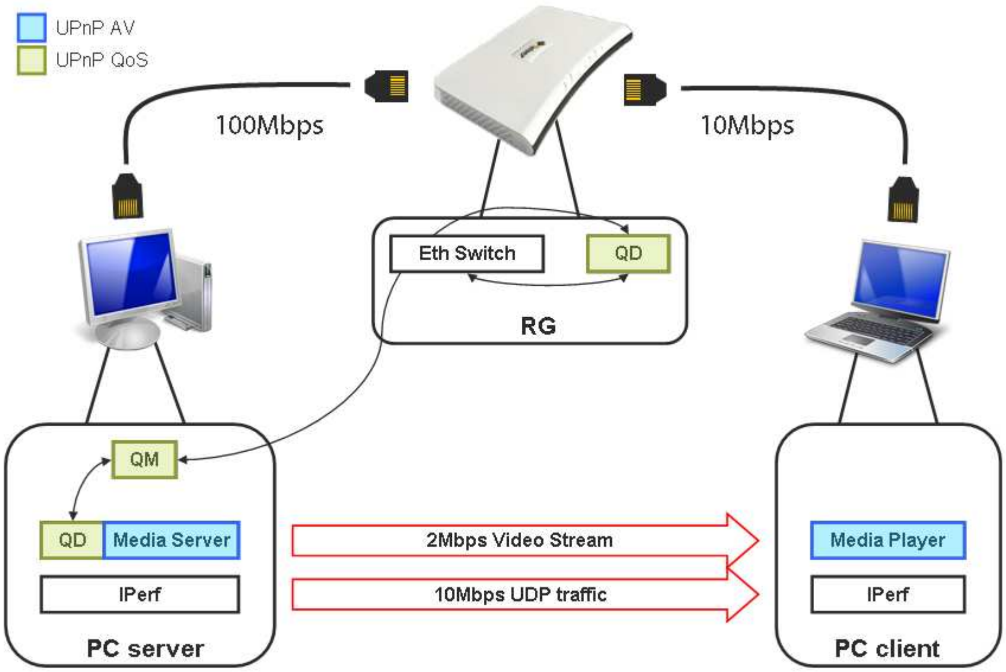


Figure 3.20 - Telsey lab setup for UPnP QoS experiments

As can be seen from the picture, the system aims to replicate a Home Network environment that includes:

- a PC server, which is closely related to the IBBT Home Server shown in Figure 3.18; for the development phase (and therefore the preliminary testing), no QosPolicyHolder was required[6] so the PC server hosts only the QosDevice and the QosManager.
    - the QM is Java based and provided by IBBT
    - the QD is developed in C by Telsey and has been implemented to be used as an additional service of a UPnP AV Media Server device, therefore just as part of an End Device. In this case, the L2-specific implementation implies setting of TOS value within packets belonging to media content streams. Upon receiving an AdmitTrafficQos, the QD service configures the socket of related media content stream to transmit packets with selected ToS.

  The PC server hosts also IPerf in order to generate background UDP traffic to “disturb” the video stream.
- the Residential Gateway, providing connectivity to the End Devices; in this case, the RG does not provide connectivity towards the Access Network, as long as such connectivity is not required in the experimental setup. The Residential Gateway hosts a QosDevice (QD), accordingly to what is shown in Figure 3.18 and the description given in section 3.2.5; such QD is the same UPnP device that runs on the PC server with Media Server functionalities disabled in the actual setup.
- a PC client, which hosts an UPnP Media Player in order to show the video stream provided by the Media Server, and again IPerf for the background UDP traffic.

A further consideration on the setup: the interconnection between the End Devices and the RG is not made in terms of optical cables but copper ones; this is due to the fact the RG with the integrated POF

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[6] as long a sit is possible to work with hard coded values

transceivers was not available during the UPnP QoS functionalities development. However, this does not affect the validity of the obtained results.

With the described setup available, two different experimental scenarios could be devised: in the first one, the UPnP QoS functionalities are disabled, while in the second one the services are up and running.

Considering the first scenario, with no UPnP QoS, the system behaves in the following way:

- the Media Player request a video to be streamed from the Media Server to the Media Player itself; when the initial bufferisation of the stream is over, the average bitrate in the Home Network is close to 2Mbps.
- IPerf is then turned on, in order to inject in the HN a background UDP traffic of 10Mbps
- as can be seen from Figure 3.20, the link between the RG and the PC client is artificially limited to 10Mbps: therefore, when both the video stream and the UDP traffic are distributed in the network, the overall bitrate is larger than the available bitrate between the RG and the PC client.
- in such a scenario, considering the different behaviour of the UDP and TCP (the video stream) traffic, the available BW is saturated by the UDP traffic: therefore, no video data is delivered to the Media Player and the video playback ends **-** until the UDP traffic is switched off.

Therefore, in the first scenario, the user experience is highly affected by the background traffic, and to restore the previous situation the user is required to manually reconfigure the network (in this case, by suppressing the UDP traffic).

The bitrate as a function of time for the different streams is shown in Figure 3.21:

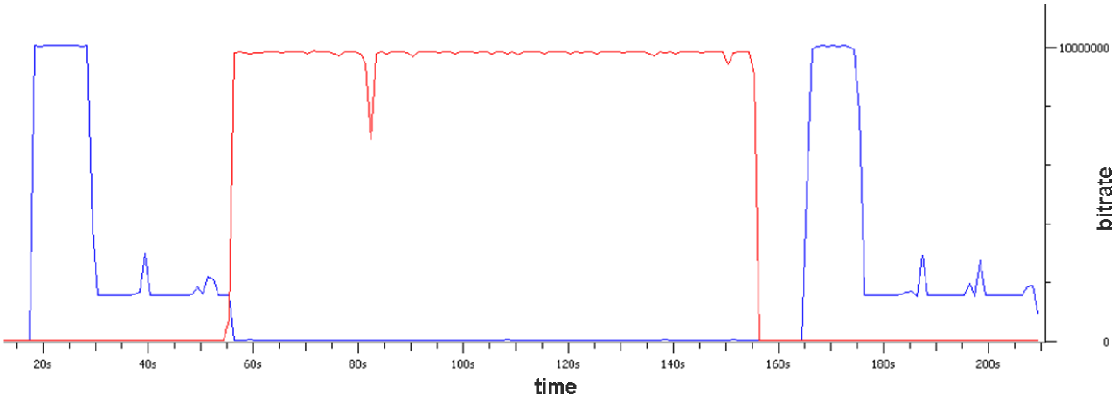


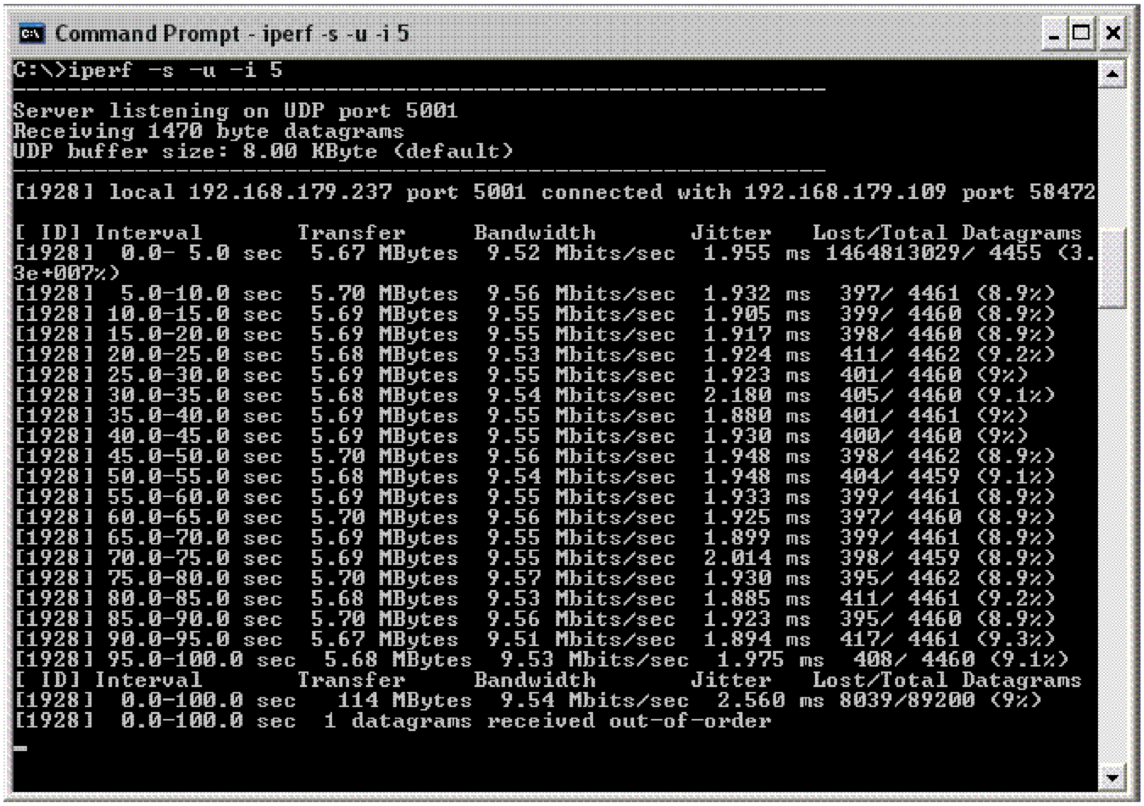
Figure 3.21 - Bandwidth allocation with no UPnP QoS (blue: TCP; red: UDP)

From the picture, it is easy to spot the bitrate evolution:

- the streaming of the video data starts at ~17s
- from ~17s up to ~30s the Media Player plays and bufferizes the data, therefore all the available BW (10Mbps) is used
- starting at ~30s, the bufferization ends and the video streams stabilizes at ~2Mbps
- at ~55s, the UDP background traffic starts: all the 10Mbps are saturated by UDP packets, and TCP traffic ceases
- from the user point of view, the video playback does not stop at 55s, but it continues as long as there is still data in the Media Player buffer; however, after nearly 50 seconds, the playback ends.

- when the UDP traffic ends, the Media player resumes bufferization and playback.

In Figure 3.22 is shown the BW occupation for the UDP traffic that confirms that such traffic saturates all the available link capability:



```
C:\>iperf -s -u -i 5
------------------------------------------------------------
Server listening on UDP port 5001
Receiving 1470 byte datagrams
UDP buffer size: 8.00 KByte (default)
------------------------------------------------------------
[1928] local 192.168.179.237 port 5001 connected with 192.168.179.109 port 58472

[ ID] Interval       Transfer     Bandwidth       Jitter   Lost/Total Datagrams
[1928]  0.0- 5.0 sec  5.67 MBytes  9.52 Mbits/sec  1.955 ms 1464813029/ 4455 (3.
3e+007%)
[1928]  5.0-10.0 sec  5.70 MBytes  9.56 Mbits/sec  1.932 ms  397/ 4461 (8.9%)
[1928] 10.0-15.0 sec  5.69 MBytes  9.55 Mbits/sec  1.905 ms  399/ 4460 (8.9%)
[1928] 15.0-20.0 sec  5.69 MBytes  9.55 Mbits/sec  1.917 ms  398/ 4460 (8.9%)
[1928] 20.0-25.0 sec  5.68 MBytes  9.53 Mbits/sec  1.924 ms  411/ 4462 (9.2%)
[1928] 25.0-30.0 sec  5.69 MBytes  9.55 Mbits/sec  1.923 ms  401/ 4460 (9%)
[1928] 30.0-35.0 sec  5.68 MBytes  9.54 Mbits/sec  2.180 ms  405/ 4460 (9.1%)
[1928] 35.0-40.0 sec  5.69 MBytes  9.55 Mbits/sec  1.880 ms  401/ 4461 (9%)
[1928] 40.0-45.0 sec  5.69 MBytes  9.55 Mbits/sec  1.930 ms  400/ 4460 (9%)
[1928] 45.0-50.0 sec  5.70 MBytes  9.56 Mbits/sec  1.948 ms  398/ 4462 (8.9%)
[1928] 50.0-55.0 sec  5.68 MBytes  9.54 Mbits/sec  1.948 ms  404/ 4459 (9.1%)
[1928] 55.0-60.0 sec  5.69 MBytes  9.55 Mbits/sec  1.933 ms  399/ 4461 (8.9%)
[1928] 60.0-65.0 sec  5.70 MBytes  9.56 Mbits/sec  1.925 ms  397/ 4460 (8.9%)
[1928] 65.0-70.0 sec  5.69 MBytes  9.55 Mbits/sec  1.899 ms  399/ 4461 (8.9%)
[1928] 70.0-75.0 sec  5.69 MBytes  9.55 Mbits/sec  2.014 ms  398/ 4459 (8.9%)
[1928] 75.0-80.0 sec  5.70 MBytes  9.57 Mbits/sec  1.930 ms  395/ 4462 (8.9%)
[1928] 80.0-85.0 sec  5.68 MBytes  9.53 Mbits/sec  1.885 ms  411/ 4461 (9.2%)
[1928] 85.0-90.0 sec  5.70 MBytes  9.56 Mbits/sec  1.923 ms  395/ 4460 (8.9%)
[1928] 90.0-95.0 sec  5.67 MBytes  9.51 Mbits/sec  1.894 ms  417/ 4461 (9.3%)
[1928] 95.0-100.0 sec  5.68 MBytes  9.53 Mbits/sec  1.975 ms  408/ 4460 (9.1%)
[ ID] Interval       Transfer     Bandwidth       Jitter   Lost/Total Datagrams
[1928]  0.0-100.0 sec   114 MBytes  9.54 Mbits/sec  2.560 ms 8039/89200 (9%)
[1928]  0.0-100.0 sec  1 datagrams received out-of-order
_
```

Figure 3.22 - UDP traffic bitrate with no UPnP QoS

In the second scenario instead the UPnP QoS is enabled; when the Media Player requests the video stream to the Media Server, the QosManager performs the set of operations described in Figure 3.19 in order to setup a QoS link between the PC server and the PC client.

In Figure 3.23 is shown the UPnP QoS test application provided by IBBT that reports all the QoS devices available on the network; as can be seen in the upper part of the picture, 2 QDs are found, while in the lower parts details are shown on the QosDevice hosted on the Residential Gateway (please spot the QD Friendly Name). All this information is dynamically retrieved.

urn:upnp-org:serviceId:QosDevice
urn:upnp-org:serviceId:QosDevice

Service Type: urn:schemas-upnp-org:service:QosDevice:3
Service ID: urn:upnp-org:serviceId:QosDevice
Device Type: urn:schemas-upnp-org:device:MediaServer:1
Friendly Name: ALPHA RG
Manufacturer: Telsey
Manufacturer URL: http://www.telsey.com/
Model Description: Telsey Digital Media Server Access Device
Model Name: CPVA642
Model Number: CPA-ZNTE7
Model URL: http://www.telsey.com/
Serial Number: TLSY-DMS-020
UDN: uuid:898f9738-d930-1db4-a3cf-00219611b4d4
UPC:

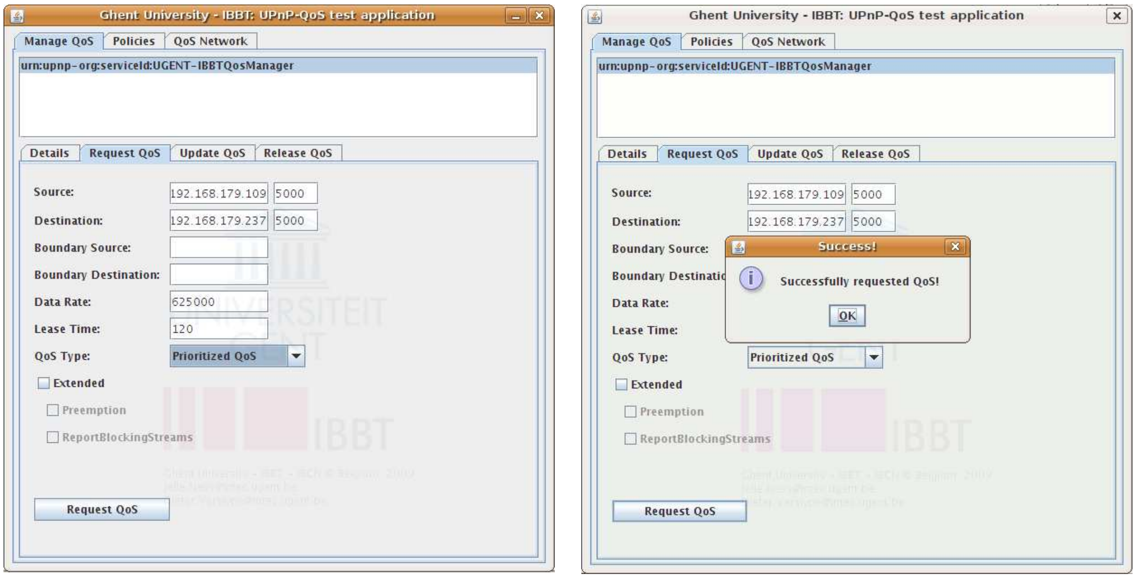
Figure 3.23 - Information retrieved form the RG QosDevice

Considering the L2 queueing mechanism described in the previous section, the following happens:

- the QM requests both the QD on the PC server and on the RG to setup a QoS for the video stream
- the QD on the PC server perform a TOS tagging of the TCP packets of the video stream
- the QD on the RG assigns the tagged TCP packets to the high priority queue (queue 1) for the required port of the Ethernet Switch, while all the other traffic is assigned to a lower priority queue (configurable, during the test was queue 4).

In Figure 3.24 is shown the QoS request performed by the QosManager; on the left side of the picture, the IBBT application prior to perform the request, showing Source and Destination IP Addresses, alongside with the QoS Type required; as stated before, due to HW limitations on the RG, only

Prioritized QoS is currently supported. On the right side of the picture, the QM informs the user all the required actions for setting up the QoS were successful and the QoS service is up and running.



urn:upnp-org:serviceId:UGENT-IBBTQosManager

Source: 192.168.179.109 5000

Destination: 192.168.179.237 5000

Boundary Source:

Boundary Destination:

Data Rate: 625000

Lease Time: 120

QoS Type: Prioritized QoS

☐ Extended

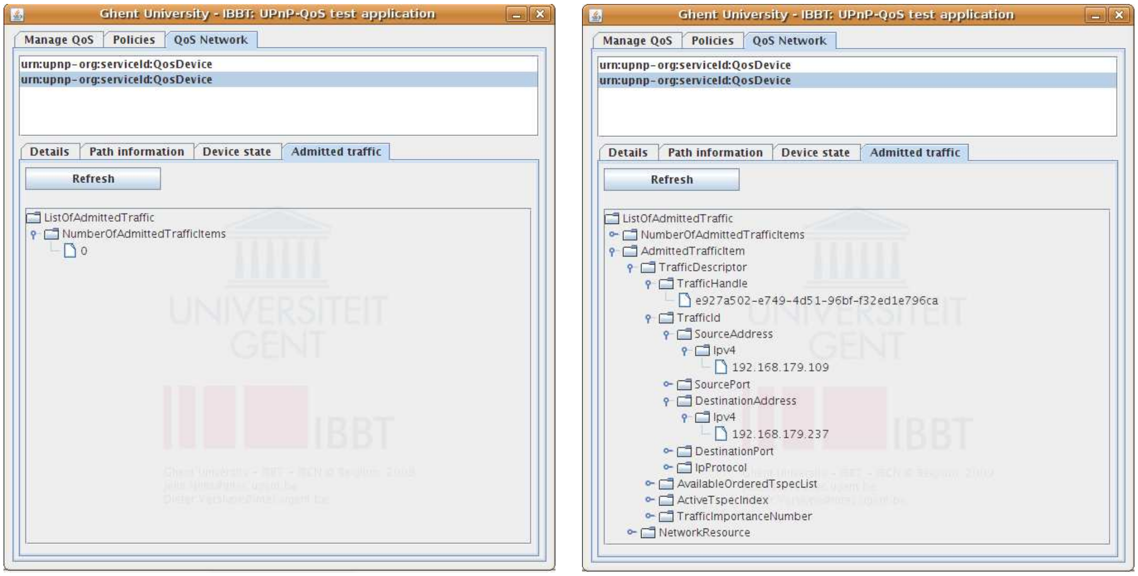
☐ Preemption

☐ ReportBlockingStreams

Successfully requested QoS!

Figure 3.24 - QoS request performed by the QosManager

Figure 3.25 shows information of the Admitted Traffic; on the left side, the scenario prior to the QoS request shows that no traffic is admitted (NumberOfAdmittedTrafficItems=0), while on the right side is shown the status of the QosNetwork after the successful QoS request, with details concerning the admitted traffic such as TrafficHandle, SourceAddress, DestinationAddress.



urn:upnp-org:serviceId:QosDevice
urn:upnp-org:serviceId:QosDevice

```
ListOfAdmittedTraffic
  NumberOfAdmittedTrafficItems
    0
```

```
ListOfAdmittedTraffic
  NumberOfAdmittedTrafficItems
  AdmittedTrafficItem
    TrafficDescriptor
      TrafficHandle
        e927a502-e749-4d51-96bf-f32ed1e796ca
      TrafficId
        SourceAddress
          Ipv4
            192.168.179.109
        SourcePort
        DestinationAddress
          Ipv4
            192.168.179.237
        DestinationPort
        IpProtocol
      AvailableOrderedTspecList
      ActiveTspecIndex
      TrafficImportanceNumber
    NetworkResource
```

Figure 3.25 - Information on the Admitted Traffic

After the setup of such a QoS connectivity, the video stream starts to flow in the Home Network; when the UDP traffic is injected, the TCP video traffic goes unaffected, due to the different prioritization performed by the QDs.

This behaviour is clearly shown in Figure 3.26:

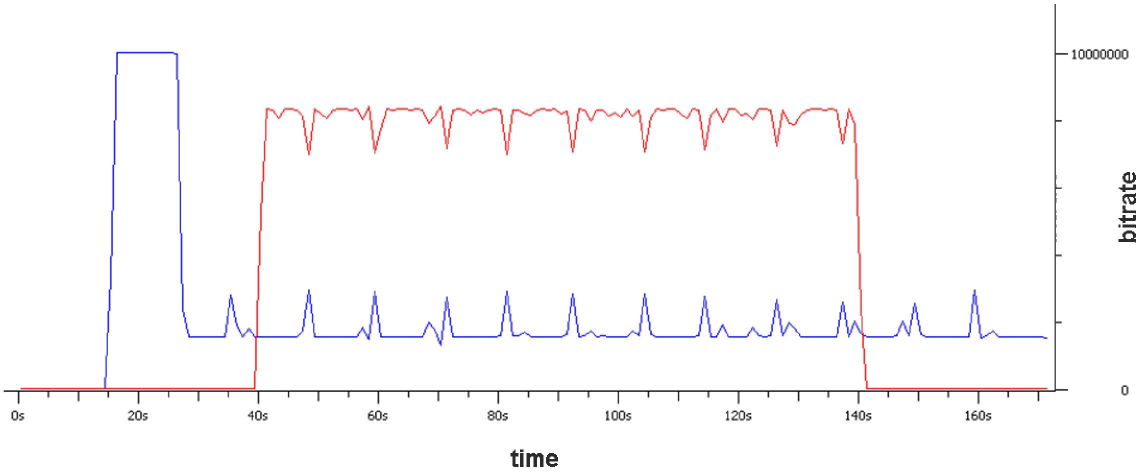


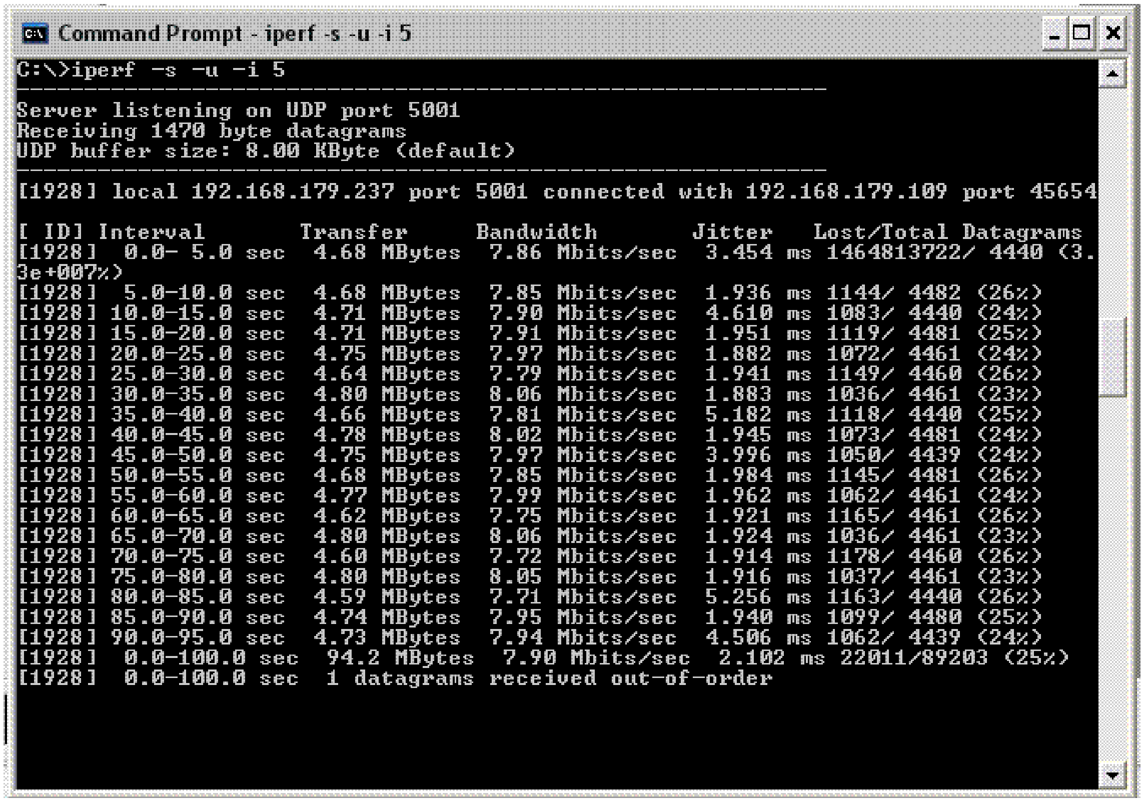
Figure 3.26 - Bandwidth allocation with UPnP QoS (blue: TCP; red: UDP)

As can be seen from the picture, the bitrate behaves as follows:

- at ~15s the Media Player requests the video data from the Media Server, and the bufferization phase starts
- from ~15s up to ~28s the Media Player plays and bufferizes the data, therefore all the available BW (10Mbps) is used
- starting at ~28s, the bufferization ends and the video streams stabilizes at ~2Mbps. Up to this point the system behaves exactly as in the previous case, as expected.
- at ~40s the UDP traffic starts; as can be clearly seen, the traffic does not saturate the available BW, but goes up to ~8Mbps
- furthermore, when peaks in the TCP traffic occur, it is possible to see that the UDP BW occupation decreases accordingly.

In this scenario, from the user point of view, the video playback does not stop and continues unaffected by the presence of the background UDP traffic.

For sake of completeness, in Figure 3.27 is shown the BW occupation for the UDP: as can be seen, the UDP traffic is limited to ~8Mbps due to the QoS.



```
C:\>iperf -s -u -i 5
------------------------------------------------------------
Server listening on UDP port 5001
Receiving 1470 byte datagrams
UDP buffer size: 8.00 KByte (default)
------------------------------------------------------------
[1928] local 192.168.179.237 port 5001 connected with 192.168.179.109 port 45654

[ ID] Interval       Transfer     Bandwidth       Jitter   Lost/Total Datagrams
[1928]  0.0- 5.0 sec  4.68 MBytes  7.86 Mbits/sec  3.454 ms 1464813722/ 4440 (3.
3e+007%)
[1928]  5.0-10.0 sec  4.68 MBytes  7.85 Mbits/sec  1.936 ms 1144/ 4482 (26%)
[1928] 10.0-15.0 sec  4.71 MBytes  7.90 Mbits/sec  4.610 ms 1083/ 4440 (24%)
[1928] 15.0-20.0 sec  4.71 MBytes  7.91 Mbits/sec  1.951 ms 1119/ 4481 (25%)
[1928] 20.0-25.0 sec  4.75 MBytes  7.97 Mbits/sec  1.882 ms 1072/ 4461 (24%)
[1928] 25.0-30.0 sec  4.64 MBytes  7.79 Mbits/sec  1.941 ms 1149/ 4460 (26%)
[1928] 30.0-35.0 sec  4.80 MBytes  8.06 Mbits/sec  1.883 ms 1036/ 4461 (23%)
[1928] 35.0-40.0 sec  4.66 MBytes  7.81 Mbits/sec  5.182 ms 1118/ 4440 (25%)
[1928] 40.0-45.0 sec  4.78 MBytes  8.02 Mbits/sec  1.945 ms 1073/ 4481 (24%)
[1928] 45.0-50.0 sec  4.75 MBytes  7.97 Mbits/sec  3.996 ms 1050/ 4439 (24%)
[1928] 50.0-55.0 sec  4.68 MBytes  7.85 Mbits/sec  1.984 ms 1145/ 4481 (26%)
[1928] 55.0-60.0 sec  4.77 MBytes  7.99 Mbits/sec  1.962 ms 1062/ 4461 (24%)
[1928] 60.0-65.0 sec  4.62 MBytes  7.75 Mbits/sec  1.921 ms 1165/ 4461 (26%)
[1928] 65.0-70.0 sec  4.80 MBytes  8.06 Mbits/sec  1.924 ms 1036/ 4461 (23%)
[1928] 70.0-75.0 sec  4.60 MBytes  7.72 Mbits/sec  1.914 ms 1178/ 4460 (26%)
[1928] 75.0-80.0 sec  4.80 MBytes  8.05 Mbits/sec  1.916 ms 1037/ 4461 (23%)
[1928] 80.0-85.0 sec  4.59 MBytes  7.71 Mbits/sec  5.256 ms 1163/ 4440 (26%)
[1928] 85.0-90.0 sec  4.74 MBytes  7.95 Mbits/sec  1.940 ms 1099/ 4480 (25%)
[1928] 90.0-95.0 sec  4.73 MBytes  7.94 Mbits/sec  4.506 ms 1062/ 4439 (24%)
[1928]  0.0-100.0 sec  94.2 MBytes  7.90 Mbits/sec  2.102 ms 22011/89203 (25%)
[1928]  0.0-100.0 sec  1 datagrams received out-of-order
```

Figure 3.27 - UDP traffic bitrate with UPnP QoS

4 Relation with testbeds

As described in detail in [8], there are 3 official testbeds made available to the partners of the ALPHA Project: considering the different focus of such testbeds and taking into account that the new RG functionalities described in this document are aimed to the introduction of new/improved services mainly in the Home Network domain, the testing facility of choice is the one provided by Telefónica I+D (TID).

4.1 TID testbed description

As mentioned before, all the details concerning the testbed structure and resources can be found in [8]; in the following, for sake of simplicity, the main characteristics of the test environment are recalled.

In Figure 4.1 is shown the actual layout of the facility: as can be seen, the testbed aims to replicate a small apartment, including a living room, a kitchen, a bedroom, a working area, plus a pair of outdoor sections.

Figure 4.1: TID Testbed actual layout

In Figure 4.2 is shown the network connectivity of the testbed; as can be seen from the picture, the cabling of the HN is largely made via POF cables; in such a scenario, it appears to be extremely convenient the introduction of a residential gateway equipped directly with suitable optical interfaces, such as the one described in section 3.1.

Furthermore, such a complex home scenario, devised for HD videos, is without question suitable for testing the UPnP QoS functionalities of different pieces of equipment, including the gateway as described in section 3.2.

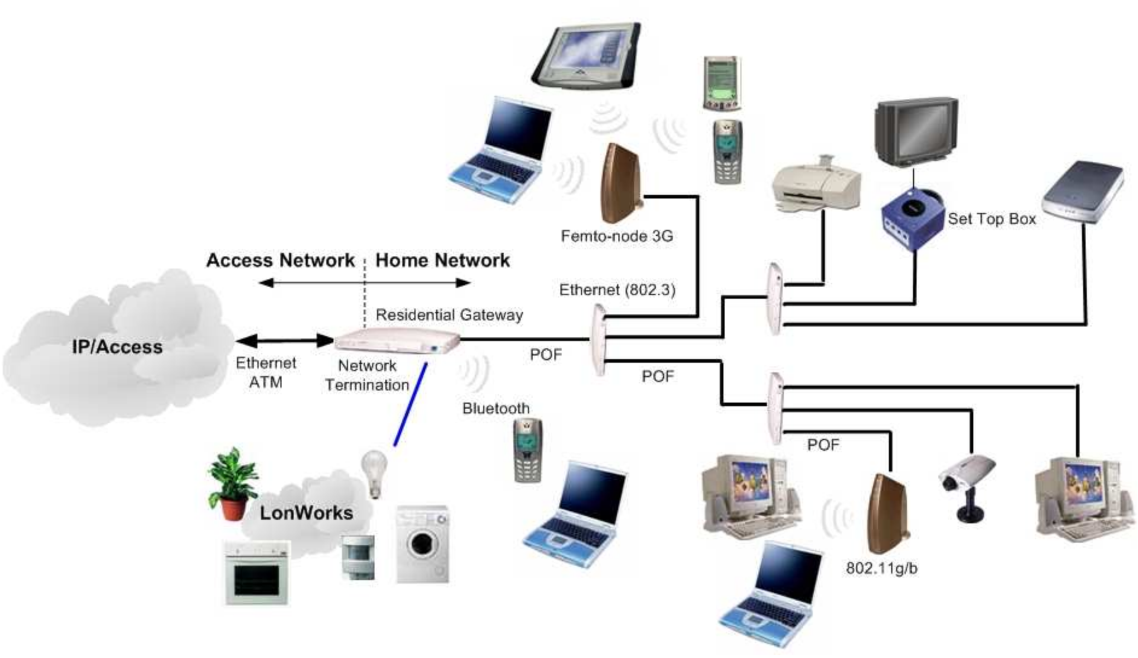


Figure 4.2: TID Testbed network connectivity

4.2 Plan for demonstrations

The preliminary experimental results reported in this document were obtained during the implementation phase of the described functionalities, carried on during 2009; such results were of course obtained in the labs of the partners were such functionalities were developed (and, to some extent, are still under development).

However, to provide a deeper characterization of the RG functionalities, it is necessary to perform dedicated tests in a more realistic scenario, such as the one provided by the described testbed.

As reported in [9], the joint experimental activity in TID testbed is foreseen for the last year of the project (2010); more in detail:

- A joint experimental activity concerning the test of a residential gateway equipped with 1Gbps POF modules will be carried out by Luceat, Telsey and TID; goal of the activity is to finalize and characterize the performances of the new functionalities developed during 2009 and reported in this document in a more realistic environment. Results for this joint activity are expected by mid 2010. The experimental result will mainly be reported in Deliverable 5.5, which will summarize the experimental activities for the third year of the project.
- A joint experimental activity concerning the test of UPnP QoS functionalities will be carried out by IBBT, HomeFibre, Telsey and TID. Goal of the activity is to evaluate the interoperability of UPnP devices provided by different manufacturers in a realistic scenario, and to evaluate the performance of UPnP QoS. The setup of the demo is foreseen for March 2010, while results are expected by mid 2010. The results will mainly be reported in deliverable 3.8, which will report results on the implementation of network reconfigurability.

5 Conclusions and Future Work

As stated in Section 1.1, the goal of this document is to provide an overview of the new network functionalities of the Residential Gateway, with a focus on the implementation aspects and the experimental results obtained by characterizing the innovative features.

The ALPHA Project Technical Annex (Annex I) states that the ALPHA specific Residential Gateway has to be implemented via the use of commercially available components; as a consequence, the ALPHA specific features will be hosted on an off-the-shelf RG platform. A review of the hardware and software specifications of the platform of choice is given in Chapter 2.

The new gateway functionalities to be implemented were chosen among the set of features described in [2] and are described in detail in Chapter 3; alongside with the description of the functionalities, some details are provided on the decision process that led to define how the functionality was to be implemented on the gateway and how such an implementation was carried out.

Following the implementation details, some preliminary experimental results are shown, mainly concerning the characterization and test of the functionalities performed during the development phase in the partners' labs, carried on during 2009.

More in details, Section 3.1 is devoted to the integration on the residential gateway of 1 Gbps POF transceivers; goal of such development is to provide high speed connectivity for the Home Network devices, following the lead of the scenarios defined in [10].

On a similar note, Section 3.2 deals with the porting of UPnP QoS functionalities on the residential gateway, in order to move toward the solution depicted in Figure 3.17, where the RG acts as UPnP QoS Manager, Device and Policy Holder therefore removing the need for an external piece of equipment providing UPnP QoS services.

As can be seen, the new functionalities of the RG are largely devoted to increasing the performances of the Home Network; therefore, it is consequent to test such functionalities in a realistic scenario that is focused on the Home Network environment; this scenario, in the ALPHA Consortium, is provided by the Telefónica testbed: Chapter 4 provides some details on the testbed, alongside with a plan for demonstrations and tests to be performed during the third year of the project (2010) and to be reported in Deliverable D5.5.